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# Design, Modeling and Analysis of Non-classical Field Effect Transistors

Peijie Feng  
*Syracuse University*

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# Abstract

Transistor scaling following per Moore's Law slows down its pace when entering into nanometer regime where short channel effects (SCEs), including threshold voltage fluctuation, increased leakage current and mobility degradation, become pronounced in the traditional planar silicon MOSFET. In addition, as the demand of diversified functionalities rises, conventional silicon technologies cannot satisfy all non-digital applications requirements because of restrictions that stem from the fundamental material properties. Therefore, novel device materials and structures are desirable to fuel further evolution of semiconductor technologies. In this dissertation, I have proposed innovative device structures and addressed design considerations of those non-classical field effect transistors for digital, analog/RF and power applications with projected benefits. Considering device process difficulties and the dramatic fabrication cost, application-oriented device design and optimization are performed through device physics analysis and TCAD modeling methodology to develop design guidelines utilizing transistor's improved characteristics toward application-specific circuit performance enhancement. Results support proposed device design methodologies that will allow development of novel transistors capable of overcoming limitation of planar nanoscale MOSFETs.

In this work, both silicon and III-V compound devices are designed, optimized and characterized for digital and non-digital applications through calibrated 2-D and 3-D TCAD simulation. For digital functionalities, silicon and InGaAs MOSFETs have been investigated. Optimized 3-D silicon-on-insulator (SOI) and body-on-insulator (BOI) FinFETs are simulated to demonstrate their impact on the performance of volatile

memory SRAM module with consideration of self-heating effects. Comprehensive simulation results suggest that the current drivability degradation due to increased device temperature is modest for both devices and corresponding digital circuits. However, SOI FinFET is recommended for the design of low voltage operation digital modules because of its faster AC response and better SCEs management than the BOI structure. The FinFET concept is also applied to the non-volatile memory cell at 22 nm technology node for low voltage operation with suppressed SCEs.

In addition to the silicon technology, our TCAD estimation based on upper projections show that the InGaAs FinFET, with superior mobility and improved interface conditions, achieve tremendous drive current boost and aggressively suppressed SCEs and thereby a strong contender for low-power high-performance applications over the silicon counterpart. For non-digital functionalities, multi-fin FETs and GaN HEMT have been studied. Mixed-mode simulations along with developed optimization guidelines establish the realistic application potential of underlap design of silicon multi-Fin FETs for analog/RF operation. The device with underlap design shows compromised current drivability but improve analog intrinsic gain and high frequency performance. To investigate the potential of the novel N-polar GaN material, for the first time, I have provided calibrated TCAD modeling of E-mode N-polar GaN single-channel HEMT. In this work, I have also proposed a novel E-mode dual-channel hybrid MIS-HEMT showing greatly enhanced current carrying capability. The impact of GaN layer scaling has been investigated through extensive TCAD simulations and demonstrated techniques for device optimization.

# **Design, Modeling and Analysis of Non-classical Field Effect Transistors**

By

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M.Sc., Syracuse University 2009

B.Eng., South China University of Technology 2007

Dissertation

Submitted in partial fulfillment of the requirements for the  
degree of Doctor of Philosophy in Electrical and Computer Engineering  
in the Graduate School of Syracuse University

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*To my grandparents, Jiabin Feng and Bangyou Tan*

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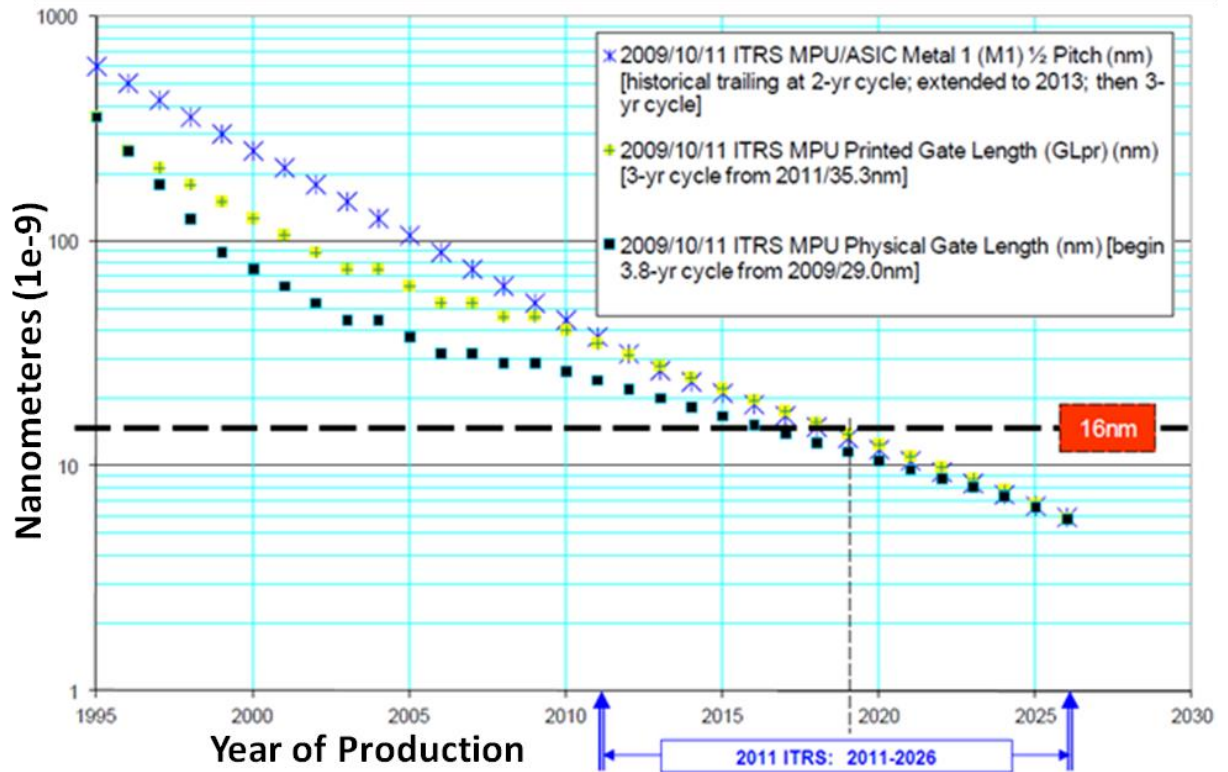
# Chapter 1

## Introduction

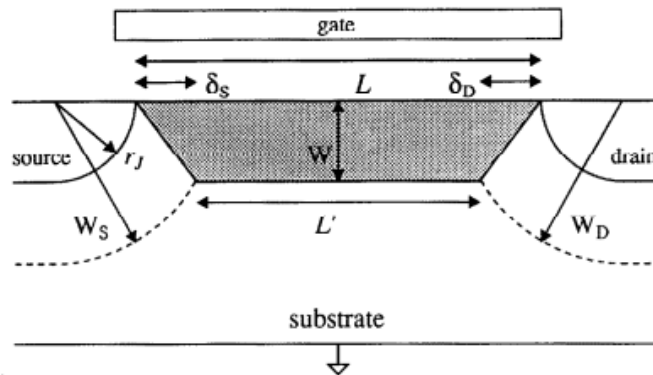
### 1.1 Moore's Law and the Roadmap

Moore's Law, serving as a guideline of integrated circuit (IC) long-term planning and development since 1965, describes the evolution of the number of transistors per chip and stimulates semiconductor academic research and industrial innovation [1]. Although the prediction has been proved to be in consistent with the transistor density growth trend over decades, the increase rate is expected to be lowered down from 2X every roughly 24 months to a 3-year cycle as shown in Figure 1.1 [2]. The change in the period is due to the challenges imposed by device dimension shrinking, especially as the technology node approaching the physics limit of the silicon device [3]. This continuous scaling of the source-to-drain distance inside the nanometer scale Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) is aimed to reduce the power consumption and enhance the operation speed [4] but it also worsens the leakage and weakens the gate controllability over the channel electrostatic potential that may offset scaling benefits [5]. To reduce the source-to-drain leakage and strengthen the gate control of the channel in planar MOSFET, high concentration bulk doping and thin gate insulator are introduced. However, the former will degrade the carrier mobility and increase the gate induced drain leakage whereas the latter permits the carrier tunneling leading to the gate leakage [6]. In addition, to minimize the side effects from random dopant fluctuation and oxide thickness

variation, both the doping development and the gate insulator deposition requires precise control of process, which plagues the fabrication complexity [6, 7].



**Figure 1.1: Evolution of Moore's Law in International Technology Roadmap for Semiconductor (ITRS) [2]**



**Figure 1.2: Scaling enlarges space charge regions and reduces the trapezoidal depleted volume (shaded) control by the gate [8]**

The reduction in device dimension causes serious capacitive coupling between source and drain to the channel potential as shown in Figure 1.2. And this detrimental effect



competes against the gate control and thereby leading to a series of side effects degrading device performance and setting the barriers to Moore's law. Those detrimental physical phenomena summarized as Short Channel Effects (SCEs) exhibit several deteriorations: (1) serious leakage current increases leakage power consumption; (2) large subthreshold slope slows down the transition between on- and off- states and reduces the switch efficiency; (3) threshold voltage roll-off results in smaller threshold voltage in shorter gate MOSFET due to charge sharing between the gate and source and drain terminals; (4) unwanted Drain Induced Barrier Lowering (DIBL) indicating the modulation of drain bias on threshold voltage due to the terminals charge sharing because of the close proximity between source and drain due to scaling; (5) degraded velocity-field characteristics due to interface scattering, phonon scattering and impurity ion scattering [5, 9-13].

To overcome those barriers to the device sizing, novel device structures and process techniques were proposed. In the early 1990, Fujitsu, IBM and Honeywell filed patent on the method of fabricating silicon-on-insulator structure (SOI), which was introduced at around 45 nm technology node mass production. As IBM and AMD claimed, the SOI structure could enhance drive current, reduce parasitic capacitance and significantly suppress susceptibility to soft errors [14]. Meanwhile, the IBM alliance's major competitor Intel, who preferred the bulk MOSFET structure, pioneered "high-k/metal gate" (HKMG) in its semiconductor fabrication process to replace the conventional silicon dioxide gate insulator and polysilicon gate for strengthened gate controllability [15]. The high-k material not only prevented the gate leakage but also allowed further shrinking of the gate dielectric layer whereas the metal gate electrodes eliminated the

undesired polysilicon gate depletion effect avoiding the threshold voltage variation [16]. This performance improvement by HKMG gate stack was later confirmed by IBM and joint partners, who adopted the stack in their 32 nm product in 2008 as well [17].

Even with those advanced techniques, Moore's Law still encounters difficulties entering sub 32-nm technology node [18]. In that regime, the gate length is so small that drain aggressively competes with gate in the regulation of the channel and thereby SCEs become more serious and greatly affect the device characteristics in the conventional MOSFET. Therefore, to maintain the miniaturization trend of the physical feature sizes of the digital functionalities (logic and memory storage), novel structures and materials are desired for Moore's law to survive in the new era "More Moore" as shown in Figure 1.3 [19].

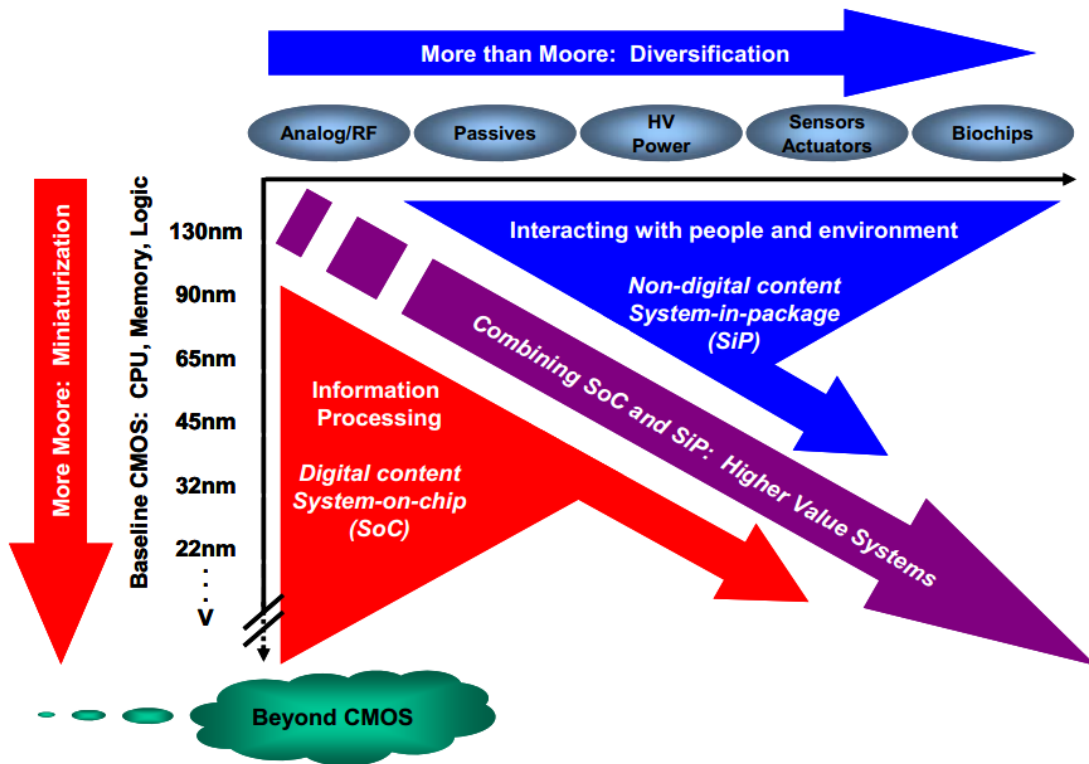


Figure 1.3: The dual trend in the ITRS s: miniaturization of the digital functions ("More Moore") and functional diversification ("More than Moore") [19]

Besides the scaling trend driven by Moore's law in the "More Moore" domain for digital functionalities, the semiconductor industry is also faced with the increasing importance of power electronics requirements of high voltage and power technologies, Radio Frequency and Analog/Mixed-Signal (RF and AMS) applications boosted by the prosperous wireless communications market, etc. Those diversified non-digital technologies are involved with the conventional silicon devices fueled by Moore's law, Complementary-Metal-Oxide-Semiconductor (CMOS) process compatible devices, and III-V compound devices which are neither compatible to the traditional fabrication nor necessarily follow Moore's Law scaling rate [19]. Tremendous efforts have also been put on the innovation of those devices for functional diversification. This direction of the progress (also shown in Figure 1.3) is labeled as another trend "More than Moore" as stated in the White Paper in 2010 ITRS. However, the roadmap development based on "More than Moore" is still in the preliminary stage due to the manufacture immaturity and the unknown device potential, and the uncertain link between markets and devices, which all require further research and investigation.

To summarize, Moore's Law is highly ordered, timely, and deliberate fashion fueling the semiconductor industry to sustain the virtuous cycle of silicon device. The dual trends "More Moore" and "More than Moore" are the derivatives of it in terms of the increased demands of functionalities. The trend "More Moore" incorporate new device structure and process techniques to support Moore's Law in the deep-nanometer regime while the trend "More than Moore" emphasizing functional diversifications concentrates on the non-digital functionalities such as RFAMS, power, sensing applications where the compound semiconductor materials are the principal candidates. In spite of the different

focus, the roadmapping of future semiconductor technologies require R&D efforts in identifying the knowledge gaps in physics barrier and in proposing solutions in technical engineering. Besides, the heterogeneous integration of different functionalities in the same chip is also desirable for future systems with diversified functions [2, 19].

## 1.2 Future Generation Devices

Novel device structures and new materials, along with improved process techniques are in high demand to maintain the self-fulfilling prophecy in the semiconductor field. The proposed next generation transistor by ITRS to fit the “More Moore” and “More than Moore” trends includes the 3-D structure silicon device, the new channel material device and the gate-stack material device as shown in Figure 1.4. In this work, the focus is on the non-planar structure multi-gate silicon and device, and new material devices: Indium Gallium Arsenide (InGaAs) FET and gate-stack Gallium Nitride (GaN) FET.

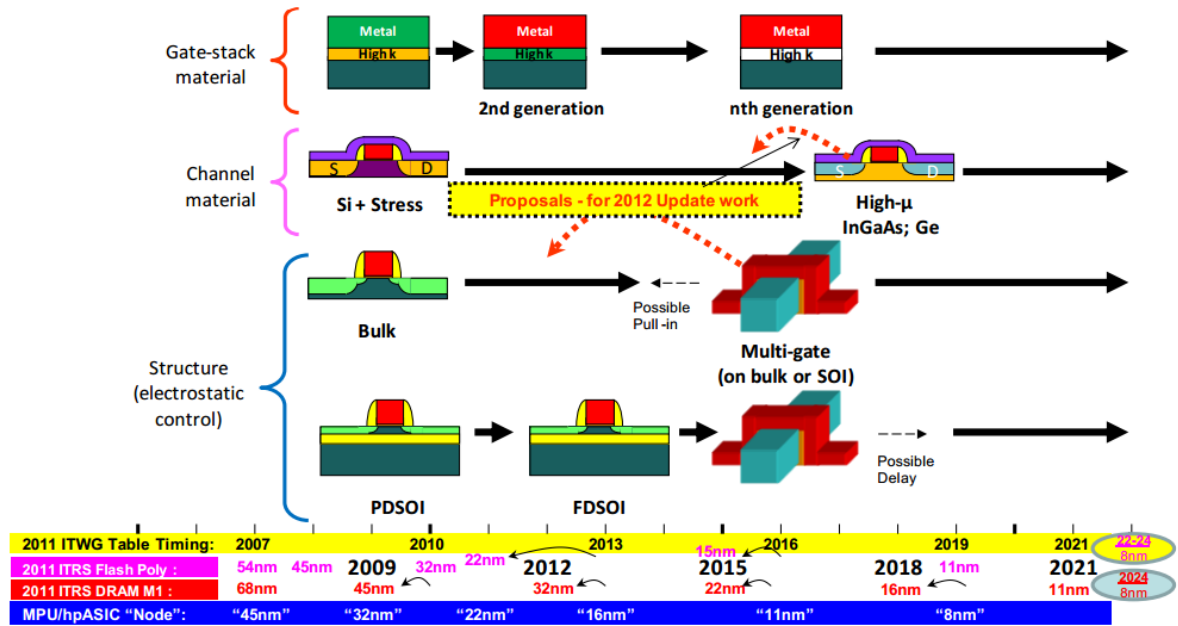


Figure 1.4: Future semiconductor devices in the ITRS roadmap [20]

### 1.2.1 The Evolution of Device Structures

The MOSFET principle was recognized in the 1920's. But the first MOSFET fabricated with silicon substrate and SiO<sub>2</sub> dielectric was realized in 1960. Three years later, the CMOS consisting of both n-channel and p-channel MOSFETs was invented. It is considered a major breakthrough in circuit and system. And it has been dominating the digital electronics since the middle of 1980s. The first MOSFET-based micro-processor appeared in the market in 1971. From that time, Moore's Law forces the size reduction for almost 50 years. Various significant changes have been made but the planar structure, which is favored for its maturity in fabrication and lower cost in production, still survives until the 22 nm technology node [21].

In the-state-of-art MOSFET transistor, the very close proximity between the source and drain requires enhanced gate control of the bulk to suppress the unwanted short channel effects. The planar structure introduces SOI and HKMG gate stack for gate controllability improvement. Those techniques were demonstrated effective but in the deep-nanometer era continuous device width sizing demands dramatic changes for the growth of the cutting-edge ICs. The 3D structure, combining parallel silicon fins to multiply drive current with reduced short channel effects is the most promising candidate to satisfy the needs.

The 3D MOSFET structures include tri-gate MOSFET, double-gate MOSFET, gate-all-around FET and nanowire. These derivatives originate from the first 3D structure FinFET which was proposed and demonstrated by Berkeley researchers in 1996 and 1999 respectively. The term fin indicates a nonplanar body which vertically positions on the surface of the substrate and wraps the conducting channel. FinFET is used somewhat generically to describe any fin-based, multi-gate transistor architecture regardless of

number of gates [22]. However, depending on the number of gate and the fin shape, the abovementioned multi-gate structure and nanowire are developed for the improvement of gate control and short channel effects suppression but at the possible increased cost and difficulty in fabrication [1].

### **1.2.2 The Emerging New Materials**

The rising III-V compound semiconductor materials, which own superior transport properties, high breakdown electric fields or high thermal and/or high heat capacity and thermal conductivity, are suitable for applications that are driven more by performance and less by cost such as high power and high frequency application and where silicon technology cannot meet the performance requirements such as high dynamic range or low noise figure [2].

In the past, the utilization of III-V semiconductor confronts the unavailability of the substrate, the lack of the appropriate gate dielectric for good interface condition, the absence of reliable enhancement-mode device, and the difficulty in the heterogeneous integration of III-V compound with silicon CMOS on the same substrate [2]. However, as the aggressive scaling pushing the silicon to its limit, scientists and researchers have been actively investigating the device physics behind the new materials, advancing new techniques for III-V substrate development and fine epitaxial growth quality. Besides, the efforts of the silicon device fabrication progress also benefit the III-V compound process techniques.

As the research and development endeavors to the semiconductor compounds over decades, InGaAs and GaN compound materials are recognized as the promising candidates in the semiconductor roadmap as the replacement materials of the silicon. The

former, featuring high electron mobility and comparable bandgap to silicon, is encouraging for ultra-high speed, ultra-low power and ultra-high frequency applications [23]. Thereby InGaAs attracts the semiconductor industry for the use in CMOS beyond the silicon theoretical limit in sub-22 nm technology regime [23-26]. The latter, owning high breakdown electrical field and high electron mobility, shows great potential in RF transistor, power amplifier and high voltage switching device applications [27].

It is expected that compound semiconductors will continue to advance through a combination of gate length scaling and more importantly epitaxy or bandgap engineering. Furthermore, new approaches in the integration of high performance III-V transistors and high-density digital circuitry are also being explored for high performance chips which are equipped with diversified functionalities that are out of reach for the conventional silicon technologies.

### **1.3 The Scope of this Work**

This dissertation presents design, simulation and analysis of non-classical silicon and III-V compound FETs for digital, analog/RF and power applications. Detailed and extensive TCAD simulations are carried out for 3-D FinFET devices and key parameters are identified for FinFET-based circuits. Compound semiconductor devices are also designed, simulated and evaluated. A novel enhancement-mode high electron mobility transistor (also known as Heterostructure FET, HFET) is proposed which significantly increases the drive current and thereby the power efficiency. The dissertation is organized into seven chapters.

Chapter 1 reviews the challenges and barriers of the semiconductor device development for different functionalities. Solutions including process techniques, new materials and novel structures are also introduced.

In Chapter 2, TCAD methodology of virtual semiconductor device development is presented. The silicon FinFET principle and design considerations in TCAD are taken as an example to illustrate the design and simulation flow of semiconductor devices.

Chapter 3 focuses on the FinFET-based digital circuit modules. FinFET structure with silicon-oxide-nitride-oxide-silicon (SONOS) stack is studied and simulated for non-volatile memory application. Meanwhile, BOI and SOI FinFETs are optimized for CMOS inverter and static random access memory (SRAM) with the consideration of self-heating effects. Performance of digital circuits consisting of these FinFETs are evaluated and compared.

Chapter 4 proposes a multi-fin FETs design technique targeted for RF applications. Overlap and underlap design configurations in base FinFET are compared first and then multi-fin device is studied to develop design limitations and to evaluate their effects on the device performance. We have also investigated the impact of the number of fins in multi-fin structure and resulting RF parameters.

Chapter 5 demonstrates a design method of E-mode N-polar GaN single-channel and dual-channel Metal-Insulator-Semiconductor (MIS) High Electron Mobility Transistor (HEMT). The mechanism behind the significant drain current carrying capability enhancement is investigated with details. The impact of GaN layer scaling on dual-channel device performance is also studied. This work was completed in Mitsubishi Electrical Research Laboratories while the author was working as a full time intern.



Chapter 6 discusses the TCAD modeling of InGaAs MOSFET. Calibrated TCDA modeling of the-state-of-the-art InGaAs planar devices with the consideration of trap effects sets the foundation in exploring the potential of InGaAs materials. Scaling of this planar III-V compound device indicates serious SCEs which can distort the function of the transistor. By introduction of non-planar structure, 3-D simulation results show that the short channel effects are suppressed while the drive current is tremendously increased.

Chapter 7 summarizes the work and provides direction for future research.

# Chapter 2

## FinFET Design Considerations in the TCAD Foundry

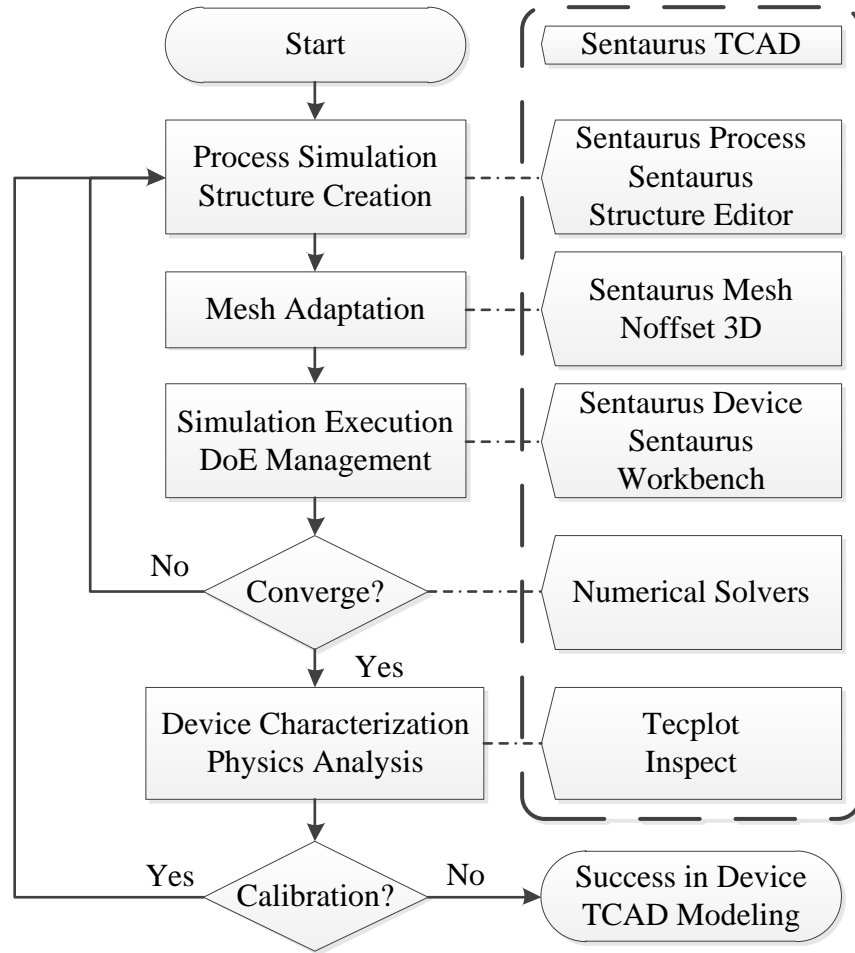
### 2.1 TCAD Methodology of Virtual Device Fabrication

Technology Computer-Aided Design (TCAD) is a branch of electronic system design software. Particularly, TCAD models semiconductor process and device physics. By computer simulation, TCAD can be used to develop and optimize semiconductor fabrication and device electrical behaviors.

TCAD is originated from bipolar technology in the late 1960s, solving the 1-D and 2-D process control issues [28]. As the advent of computer modeling of semiconductor in the 1970s and the popularity of MOSFET technologies in the 1980s, tremendous efforts were put in the development of the TCAD [29]. This electronic design automation now becomes an essential toolset and gains broad deployment as a workhorse of integral technology in both semiconductor process and device simulation.

The goal of TCAD is to offer interactive physical description and investigation of semiconductor devices by simulation and modeling to support circuit design as well as to reduce R&D time and cost. Using TCAD, conventional semiconductor device characteristics can be predicted with time and economic efficiency based on developed model and simulation algorithm, while novel process, structure and materials can be visualized through phenomenological and semi-empirical models to catch the physical insights and speed up the learning curve [30].

Current major TCAD suppliers include Synopsys, Silvaco and Crosslight. The “Sentaurus TCAD” toolset, provided by Synopsys, is a comprehensive nanoscale process, device design and simulation tools. It supports industry leading process and device simulation with a powerful GUI-driven simulation environment for managing simulation tasks and analyzing simulation results. In this dissertation, Synopsys Sentaurus TCAD is the tools used for the semiconductor device and circuit design, characterization, modeling and analysis.



**Figure 2.1: Fabricate semiconductor devices in TCAD foundry**

The design and simulation flow in Sentaurus TCAD is shown in Figure 2.1. The device geometry structure with doping profile is designed by either Sentaurus Process or

Sentaurus Structure Editor. The former is a 3-D capable process simulator for silicon semiconductor process technology development and optimization. Its comprehensive process models cover implantation, diffusion, annealing, etching, oxidation, epitaxial growth, etc. The latter is not only a 3D-capable device editor but also a 3D-capable process emulator. And geometric and process emulation operations can be mixed freely, adding more flexibility to the generation of 3D structures. The Sentaurus Structure Editor is suitable for design of non-classical devices such as novel silicon transistor and non-silicon device.

The device created by either Sentaurus Structure Editor or Sentaurus Process is a “virtual” device whose physical properties are assigned to a finite number of discrete grids of nodes. This grid adaptation procedure is completed by Sentaurus Mesh, which is a mesh generator that incorporates two mesh generation engines: an axis-aligned mesh generation engine and a tensor-product engine that produces rectangular or hexahedral elements. The choice of the appropriate mesh generator depends largely on the geometry of the device and the essential surfaces within the device. For planar devices such as conventional MOSFET and layer-stack HEMT, axis-aligned mesh generator is recommended. For device where most important surfaces are non-axis-aligned or curved, the tensor-product engine Noffset3D is adopted to produce meshes containing layers to better conform to the curved surfaces [31]. The mesh quality is controlled by the refinement information according to user requirements. Generally, a total node count of 2000 to 4000 is reasonable for most 2D simulations [32]. Large power devices or 3D structures require a considerably larger number of elements. It is noted that the mesh quality will have impact on the simulation accuracy, efficiency and robustness. A most

suitable mesh strategy should compromise fine mesh for high current density, high electric fields, high charge generation regions to ensure the accuracy and robustness, and coarse mesh to relatively low physics activity regions such as substrate and most source/drain regions for the improvement of simulation efficiency.

After the device passed by the mesh engine, next steps include applications of physics models, bias condition and numerical solution algorithm in Sentaurus Device, a comprehensive, semiconductor device simulator capable of electrical, thermal and optical device characteristics simulation [32-34]. Similar to other TCAD toolsets, Sentaurus TCAD solves fundamental equations along with its own advanced model in explaining of non-ideal device phenomena during device simulation [32]. The fundamental equations consist of Poisson's Equation relating variations in electrostatic potential to local charge densities,

$$\nabla^2 \varphi = -\frac{\rho}{\varepsilon}$$

where  $\varphi$  is the electrostatic potential,  $\varepsilon$  is the local permittivity, and  $\rho$  is the local space charge density; continuity equations which describe charge conservation with the integration of carrier transport models:

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot \vec{J}_n + G_n - R_n$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot \vec{J}_p + G_p - R_p$$

where  $q$  is the charge unit,  $n$  and  $p$  is the electron and hole concentration,  $J$ ,  $G$ ,  $R$  stand for the current density, the generation rate and the recombination rate, respectively.

Four different carrier transport models are available for the description of current density in various scenarios. The Drift-diffusion model can be selected in low-power

density long channel device isothermal simulation. The Thermodynamic model accounting for self-heating effect is suitable for device with low thermal exchange. The Hydrodynamic model can be applied in small active region device and the Monte Carlo model is capable of full band structure solution. In this work, we employ the first three carrier transport models and select the appropriate one to device simulation according to the device material, structure and operation, and interested device characteristics.

In addition to basic transport equations, TCAD modeling of semiconductor devices also need to address the band structure and the mobility properties. The band structure models are involved with bandgap, electron-affinity, effective mass and effective density-of-states. The mobility models discuss the impact of the phonon scattering, impurity ion scattering, carrier-carrier scattering and surface roughness and scattering.

When we simulate devices other than MOSFET, particular models for material and physical phenomena should be included in the simulation. For instance, the tunneling and trapping must be recorded in the simulation of a nonvolatile memory whereas spontaneous and piezoelectric model should be introduced in the investigation of heterostructure device.

Besides general simulation methods, phenomenological and semi-empirical models are often used to account for novel process, material or structure and to compromise the simulation efficiency and robustness [30]. For example, the HKGM gate stack can be modeled through changes to the equivalent oxide thickness with an additional dipole layer; the Ohmic contact on the nitride materials can be visualized as a Schottky contact with only electron tunneling to improve simulation convergence rate.

The simulation convergence as well as simulation time also depend on the iterative algorithm settings of the Newton solver. Several factors are needed to be addressed for the trade-offs among simulation efficiency, accuracy and robustness: the maximum number of iterations; the desired precision of the solution; the linear solver appropriate for interested device operation; and the introduction of damping methods in expedition of the initial solution search at the cost of result accuracy [32]. To achieve good convergence rate of simulations, efforts need to put on the compromise among physics model, mesh quality and solution algorithm [2]. It should be pointed out that examination of the simulated device physics properties such as electron density, electric field and electrostatic potential will help identify the cause to the convergence issue.

As discussed above, there is no doubt that TCAD is a powerful and rigorous single-device simulator. Furthermore, TCAD is also a mixed-mode device and circuit simulator to perform multi-device simulation. Similar to SPICE, TCAD needs to define a circuit netlist to virtually connect the active and the passive components and solve the whole system of devices. More than that, TCAD mixed-mode simulation can add more device physics details during the circuit operation and provide results more close to the real integrated circuits. In this work, we have adopted the mixed-mode TCAD simulation to evaluate FinFET digital circuit module DC performance and multi-fin FETs AC intrinsic and extrinsic performance with the consideration of the parasitic components modeling. It should be noted that the AC system simulation solving the Jacobian matrix is made up of the carrier density, the transport property and the temperature equations we have discussed before [32]. The heavy computations imply that convergence and efficiency will be the issues challenging AC simulation.

Through the careful design and setting of the simulation, modeled devices with good convergence rate will be further investigated by Design of Experiments (DoE) for calibration, fine tuning or physics properties study. Here, DoE for semiconductor process and device design refers to variation of fabrication parameters that can be applied for device development. It aids to obtain information for device characterization and optimization, to improve manufacturing processes, and to design and develop new processes and products. Proper DoE and the choice of samples for analysis are important factors that increase the likelihood of success in semiconductor device fabrication. DoE can be performed in Sentaurus Workbench, a primary graphical front end that integrates Sentaurus simulation programs into one environment. Also in the workbench, graphic visualization can be obtained through Tecplot and device characteristics variables can be extracted through Inspect.

This dissertation work will follow the above methodologies and implement three types of non-classical transistors including silicon multi-gate MOSFETs, GaN HEMTs and InGaAs devices in the Synopsys Sentaurus TCAD foundry.

## **2.2 An Introduction of FinFET**

A description of FinFET development will be presented in this chapter while the III-V material and corresponding devices will be discussed in Chapter 5 and Chapter 6 independently.

For an MOSFET transistor, generally it is expected that the channel current is very small when the device is off, rises sharply when the device is turned on, and remains constant when the device is biased in the saturation region. This desired device characteristic may be achieved in a long channel conventional MOSFET because the



source/drain has little interference on the gate control of the channel. However, the continuous scalability causes serious capacitive coupling between source and drain to the channel potential. And this detrimental effect competes with the gate control and thereby leads to short channel effects degrading device performance.

A simple tool, Voltage-Doping Transformation (VDT) model, can be used to evaluate the effects of conventional planar transistor sizing parameters on device electrical characteristics [35, 36]. The following expressions are derived from the VDT model in the particular case of the short channel effects:

$$SCE = 0.64 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left[ 1 + \frac{x_j^2}{L_{el}^2} \right] \frac{t_{ox}}{L_{el}} \frac{t_{dep}}{L_{el}} V_{bi} = 0.64 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} EI \cdot V_{bi} ,$$

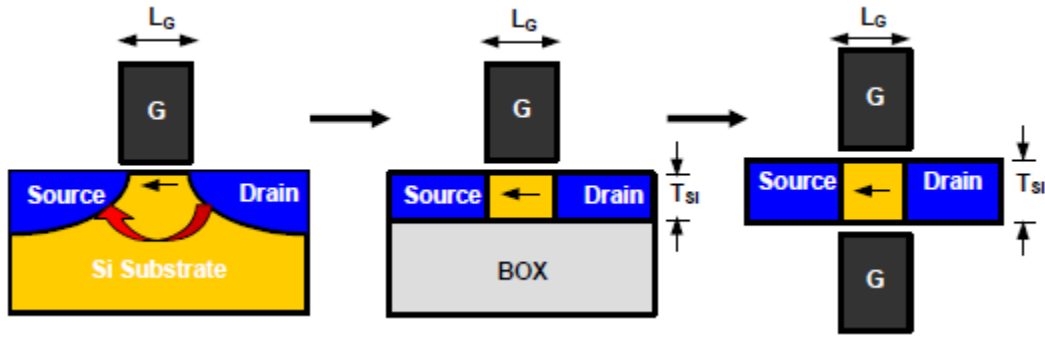
and specifically the DIBL,

$$DIBL = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \left[ 1 + \frac{x_j^2}{L_{el}^2} \right] \frac{t_{ox}}{L_{el}} \frac{t_{dep}}{L_{el}} V_{DS} = 0.80 \frac{\varepsilon_{Si}}{\varepsilon_{ox}} EI \cdot V_{DS} ,$$

where  $L_{el}$  is the effective channel length,  $x_j$  is the source and drain junction depth,  $t_{ox}$  is the equivalent oxide thickness,  $t_{dep}$  is the width of the depletion region,  $V_{bi}$  is the source or drain built-in potential,  $V_{DS}$  is the drain-to-source bias [1]. The parameter  $EI$  is short for “Electrostatic Integrity” involved with device geometry dimension and drain influence of the channel. Larger is the  $EI$ , stronger the SCEs plaguing the device performance.

The minimization of  $EI$  actually is realized by the enhancement of the gate control of the channel potential compared to the drain interference. As discussed previously, various technological innovations such as ultra-shallow source/drain junctions, high-k metal gate stack and ultra-thin bulk have been applied to the conventional MOSFET to reduce  $x_j$ ,  $t_{ox}$  and  $t_{dep}$  respectively to strengthen the gate controllability. However, those techniques are

also approaching their physical limitations as the scaling art entering sub-32 nm regime. In that nanometer scale of conventional planar device, precise doping control is required to form ultra-shallow source/drain junctions and to prevent random doping fluctuation but this seriously challenges the process techniques [37]. Also, the development of ultra-thin bulk with good uniformity still needs significant efforts in the fabrication [38]. And the scaling of gate dielectric, helping the top gate control the whole body, also encounters increased gate leakage due to direct tunneling [39].

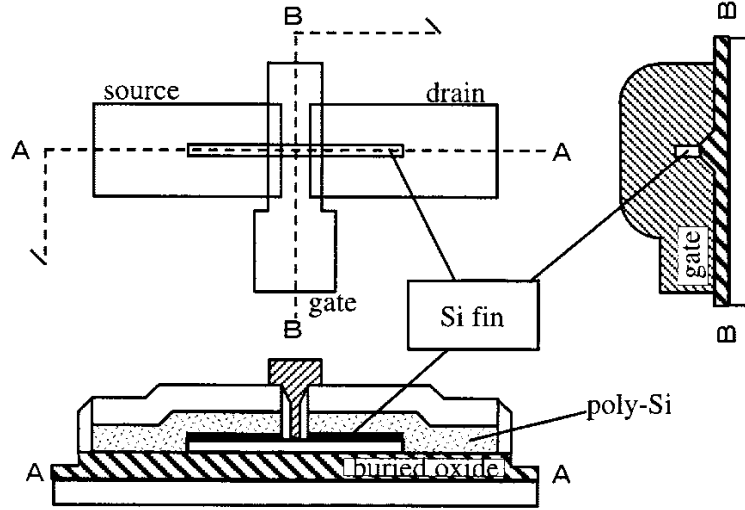


**Figure 2.2: An additional gate will improve gate management of the channel [40]**

To alleviate the pressure on the process techniques of nanometer-scale planar transistors for SCEs management, a novel structure in which an additional gate is inserted at the other side of the bulk is considered. With the enhanced gate control, bulk high doping will be eliminated and aggressive gate dielectric scaling will be decelerated.

In the 1990s, Berkeley proposed and fabricated such a non-planar MOSFET structure with a thin body controlled by the gate from more than one side [41]. The structure is shown in Figure 2.3. A thin lightly-doped Si fin serves as the body of the MOSFET and a heavily-doped poly-Si film wraps around the fin to form the electrical contact. The gap of the S/D pads is reduced by the dielectric spacer. The smallest gate achieved in this structure is 17 nm. This novel structure solves a series of scalability problems and also

demonstrates suppressed SCEs than conventional MOSFET. Besides, this superior device is compatible to the planar CMOS fabrication platform and thereby considered economically efficient.



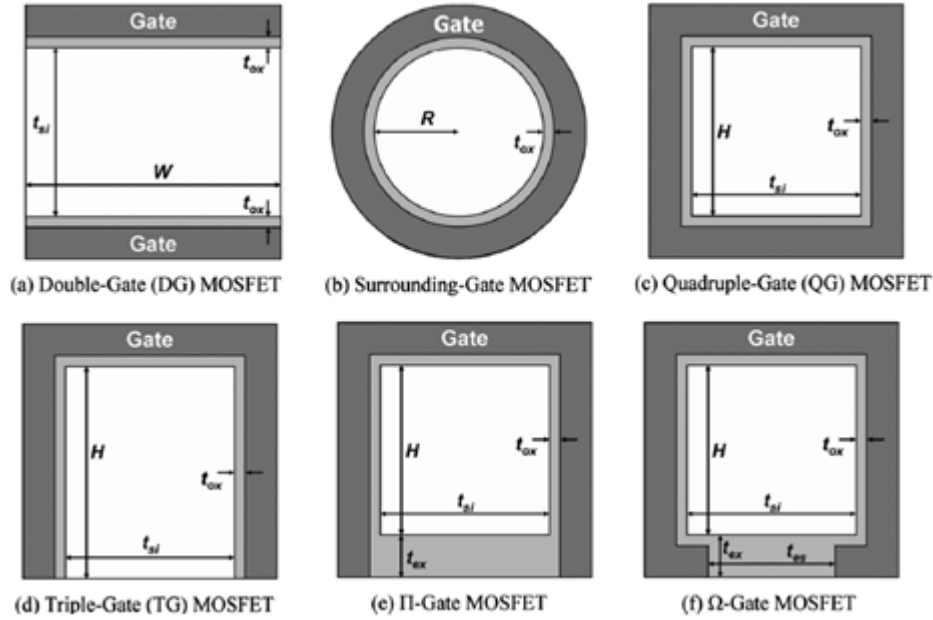
**Figure 2.3: FinFET typical layout and schematic cross sectional structure [41]**

FinFET is also demonstrated to be suitable for scaling. In the 2000s, 10, 5 and sub-5 nm FinFET preliminary samples are fabricated [42-44]. Numerous technical reports and academic papers show that scaled FinFET manifest itself with a higher  $I_{on}/I_{off}$  ratio, a lower subthreshold slope  $SS$  and an improved DIBL by the enhanced gate controllability compared to conventional planar counterpart [41, 45, 46].

### 2.3 FinFET Design Considerations

The non-planar feature of FinFET encourages the exploration of the multi-gate structure as shown in Figure 2.4. Berkeley's FinFET is a classical double gate structure where the top gate control is suspended by the thick top gate dielectric. The tripe-gate structure activates the top gate control by shrinking the corresponding gate dielectrics.  $\Omega$ -gate and  $\Pi$ -gate are also derived from this structure. Surrounding-gate MOSFET and

quadruple-gate MOSFET have the body sealed by the gate around and they are also known as nanowire.

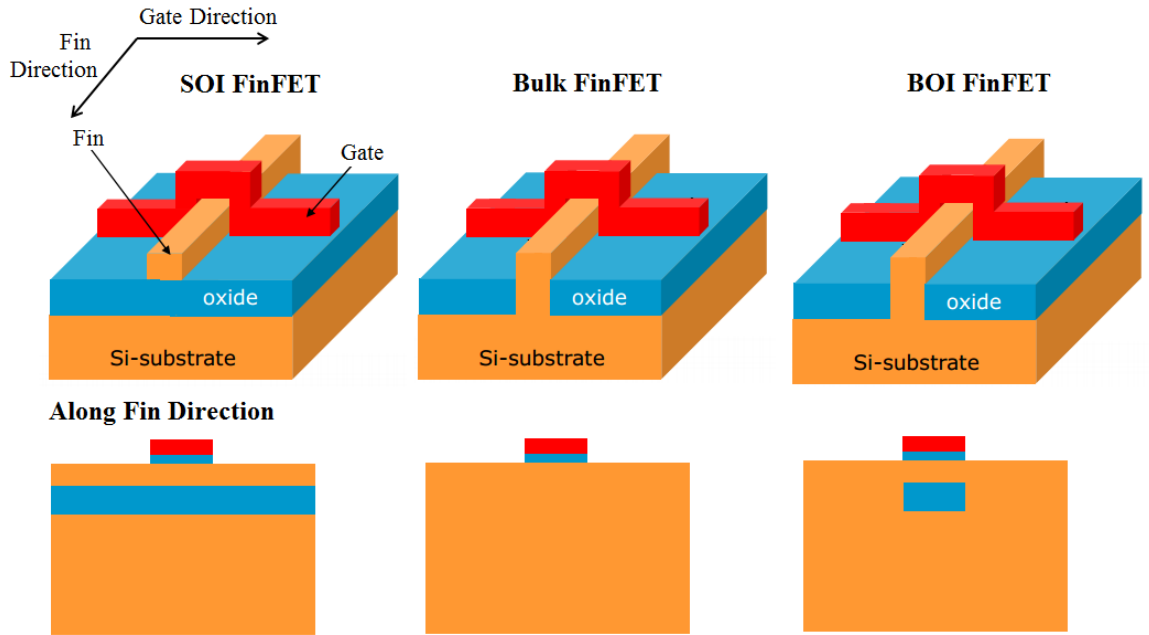


**Figure 2.4: Possible multi-gate structure of FinFET [47]**

Triple-gate and double-gate transistor are recognized as feasible structures for fabrication compared to the other four types of MOSFET. And we will implement these two devices and evaluate their potential for digital and analog/RF applications with TCAD.

Besides different gate structures, FinFET is also differentiated by different substrate integration techniques. As shown in Figure 2.5, the 3-D fin can be fabricated on silicon-on-insulator [41, 48] or by standard bulk CMOS technology [49]. The bulk FinFET structure has a lower wafer cost and wafer defect density compared to the SOI technology [50]. It also eliminates the floating body effect and improves heat dissipation [51]. In comparison, SOI FinFET demonstrates a easier fin patterning, a higher  $I_{on}/I_{off}$  ratio and a better immunity to variability issues while scaling down the dimension with a 10 nm gate length [52]. These favorable features make SOI FinFET promising towards

microprocessor performance improvement and energy conservation at 14 nm node. When different alliances have debate on either bulk FinFET or SOI FinFET, a body-on-insulator FinFET structure was proposed in 2008 [53]. It is claimed to have good heat dissipation capability by having the source and drain region directly connected to the substrate, and suppressed leakage current by burying a localized insulator below the fin body (see Figure 2.5).



**Figure 2.5: Possible substrate types of FinFET [54]**

In this dissertation work, for silicon FinFET, the focus is on both digital and non-digital functionalities at 22 nm technology node. For DC characteristics, the design considerations are on  $I_{on}/I_{off}$  ratio, short channel effects, on-state current, where leakage current, threshold voltage, subthreshold swing and DIBL are the evaluation parameters. For analog/RF figure of merits, the design guideline pays attention to current drivability, intrinsic gain, cutoff frequency and maximum frequency, where the intrinsic and extrinsic components such as channel resistance, junction capacitance and interconnection

variables are involved. Given that both digital and non-digital applications have interest in operating frequency, SOI FinFET pleases circuit designers because of its much smaller junction capacitance [55] and it is appreciated by IBM and AMD camp. Here, our own silicon FinFET reference is also with SOI FinFET technology.

The device design must follow the fabrication reality. For the device dimension design, several constraints should be addressed. For a 22 nm node FinFET, the gate length ranges from 20 to 25 nm [2]. Fin height in NMOS FinFET is set to be around 40 nm as recommended in [56]. For PMOS FinFET, the height will be approximately 1.4 times that of the NMOS to compensate the low mobility of holes [57]. The aspect ratio within FinFET (fin height to fin width,  $H_{\text{fin}}/W_{\text{fin}}$ ) is kept around 2.5 to achieve a thin fin, which allows more control over the channel potential from the gate [58]. The equivalent oxide thickness (EOT) for a high- $\kappa$  gate dielectric is around 1 nm according to the technology node requirements [2]. For the doping profile design, the interest lies in bulk region, source/drain region and extension region. The fin body is usually associated with lightly channel doping to minimize random dopant fluctuation. But for the source/drain region, heavy doping along with raised source/drain structure is applied to minimize the parasitic resistance. Only the gate extension region has freedom in doping optimization. Details will be illustrated in Chapter 4.

The FinFET will be ready for device simulation after its physical properties are discretized into a non-uniform grid (or mesh) of nodes. A suitable mesh strategy should address both simulation efficiency and robustness. The fin body surface, gate extension region, gate oxide interface will be given fine mesh since channel development, high electrical field and scattering are expected in those regions.

The meshed structure has a very small active region which requires Hydrodynamic model accounting for energy transport of the carriers and Quantization model addressing quantum correction on carrier densities and field distribution within the device. Besides, mobility model should be carefully selected to reflect the interface scattering, impurity scattering and high field velocity saturation. If temperature factor is included in the simulation, Philips Unified Mobility model and Lattice temperature variable need to be included.

Calibration is carried out through DoE with attention on threshold voltage, the magnitude order of  $I_{\text{on}}$  and  $I_{\text{off}}$  and the shape of input and output  $I$ - $V$  curves.

## **2.4 Summary**

TCAD demonstrate time and cost efficiency in modeling semiconductor process and device physics through numerical computation. It can be utilized to develop and optimize semiconductor process and simulate device electrical behaviors with DoE studies. FinFET evolution history, device physics and TCAD design considerations are also provided in this chapter.

# Chapter 3

## FinFET Application in Digital Functionalities

### 3.1 Introduction

The art of scaling, which cuts across the technological evolutions, shapes the roadmap of the semiconductor industry. In view of the digital electronics application, the scaling inspires the academia and industry to develop new techniques, search new material and invent new structure for the interest of improving the density, speed and power consumption of the most popular digital functionalities: logic and memory storage.

CMOS logic and memory modules are the major portion of semiconductor device production [2]. These circuitries are based on the fundamental inverter circuit consisting of a pair of complementary MOS (CMOS) transistors: N-channel MOSFET and P-channel MOSFET (NMOS and PMOS, where channel contains electrons and holes, respectively). Such a CMOS inverter can be utilized as a logic gate unit to establish CMOS circuit for complex logic function and to form cross-coupled inverters for memory bit storage. It should be noted that the CMOS unit has high noise immunity and low static power consumption. Therefore it is suitable for high density integration on a chip and thereby the most used technology to be implemented in Very Large Scale Integration (VLSI) technology, such as Central Processing Unit (CPU), SRAM memory chip.



Besides the CMOS based SRAM memory which has fast read access time but only temporarily stores digital information when power supply is on, there is another type of memory which is capable of permanent information storage even when the power is disconnected. According to capabilities of memory states maintaining dependent on the need of power supply, the former is labeled as one of the volatile memory while the latter is categorized into Non-Volatile Memory (NVM) [59]. The main advantage of volatile memory is in their ability to operate at a very high speed even with low-operation voltage. However, their disadvantages include its low storage density and the need of a power supply to retain information. In contrast, the non-volatile memory (NVM) can store information when not powered. This feature enables non-volatile memory to be used for the long-term persistent storage.

As we have discussed in previous chapters, as the scaling of logic and memory storage further proceeds, conventional planar device structure faces serious leakage current problem because of the weakened gate control, and threshold voltage fluctuation due to the random distribution of dopants. Fortunately, the 3D structure FinFET, along with the material and process techniques innovation such as high- $\kappa$  gate dielectric, metal gate electrodes, strain enhancement, is the promising candidate for the CMOS logic design to meet the trade-off among the transistor density, the power consumption and the operation frequency. This non-planar FinFET structure is also used to design the memory module to enhance storage capacity, reduce power consumption and increase operational speed.

In this chapter, we present construction of the basic CMOS logic gates using 3-D BOI and SOI FinFETs. These digital circuits are optimized and their electrical behaviors

are extracted under the low supply voltage bias. Then the corresponding SRAM cell for volatile storage are simulated and characterized. A brief study of FinFET NVM cell is also discussed in this chapter.

## 3.2 FinFET CMOS Inverter and SRAM Module

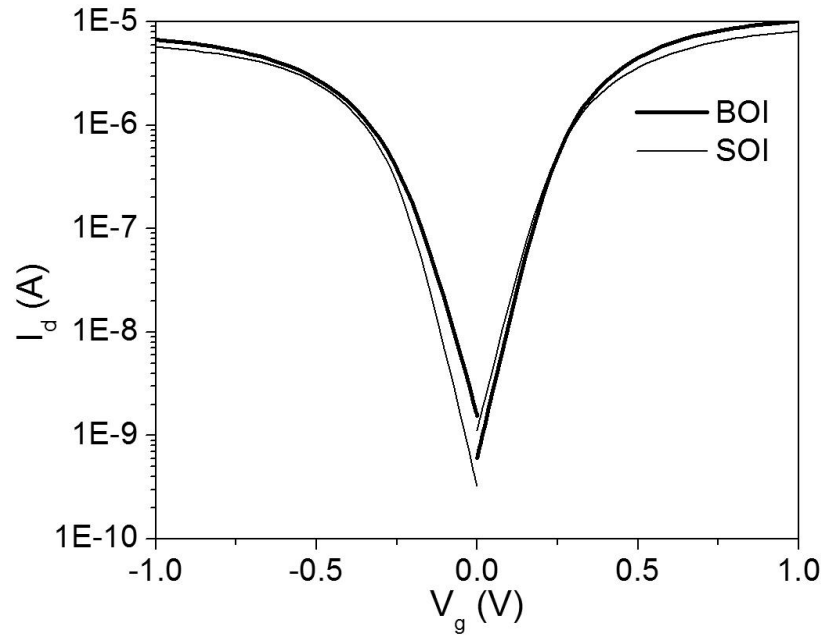
As discussed in Chapter 2, the BOI FinFET is a compromise of Bulk FinFET and SOI FinFET. It reduces the parasitic resistance and eases the self-heating issue which burdens the SOI device. It also addresses the concern of the bulk FinFET on leakage current and short-channel effects. However, the BOI device requires extra fabrication steps to bury the insulator right underneath the fin body and this increases production cost [53]. To evaluate whether the extra efforts justify the increased cost, in this chapter, we present design, simulation, and comparison of SOI and BOI FinFET based digital circuit modules.

### 3.2.1 FinFET Based CMOS Inverter

The optimized 22 nm node BOI and SOI FinFETs were designed with the suggested dimension and doping based on the DoE in Chapter 2. Both 3-D BOI and SOI FinFET are designed with 25 nm gate length, 0.9 nm equivalent oxide thickness and 50 nm fin height. The bulk is lightly doped at  $10^{15} \text{ cm}^{-3}$  and the source/drain region at  $10^{19} \text{ cm}^{-3}$ . Quantization Model, hydrodynamic transport model and Philips unified mobility model are included to consider quantum effects, temperature dependence of mobility and the lattice temperature which describe the self-heating effect (SHE).

The simulated SCEs including SS and DIBL are summarized in Table 3.1 for both SOI and BOI devices. The buried insulator and the fin structure improve SCEs. The threshold voltage characteristics for NMOS and PMOS are shown in Figure 3.1. The threshold voltage for n-Type BOI and SOI FinFET are around 0.25 V, whereas the P-type

ones are around -0.26 V. SHE degrades on-state current of SOI FinFET but has less impact on BOI device when gate bias is greater than 0.6 V. However, for low voltage applications, SHE has minimal influence on both devices [53, 60]. The comparison of output characteristics are also shown in Figure 3.2. The BOI FinFET on-state current is slightly greater than the SOI one, but its parasitic capacitance is also larger than the SOI structure [53]. These are due to the source/drain region extension and additional junctions formed at the substrate.



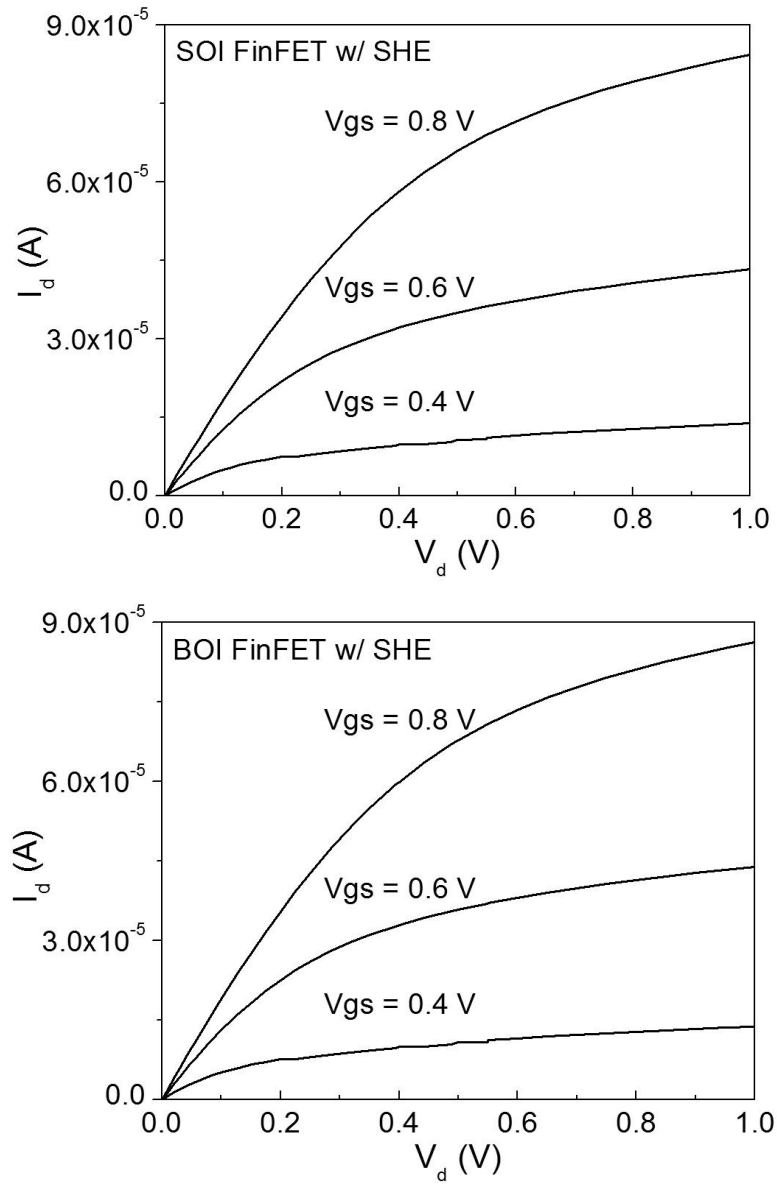
**Figure 3.1: Device input characteristics of n-type and p-type FinFET with BOI and SOI structures at 22-nm node**

**Table 3.1: Summary of device short channel effects**

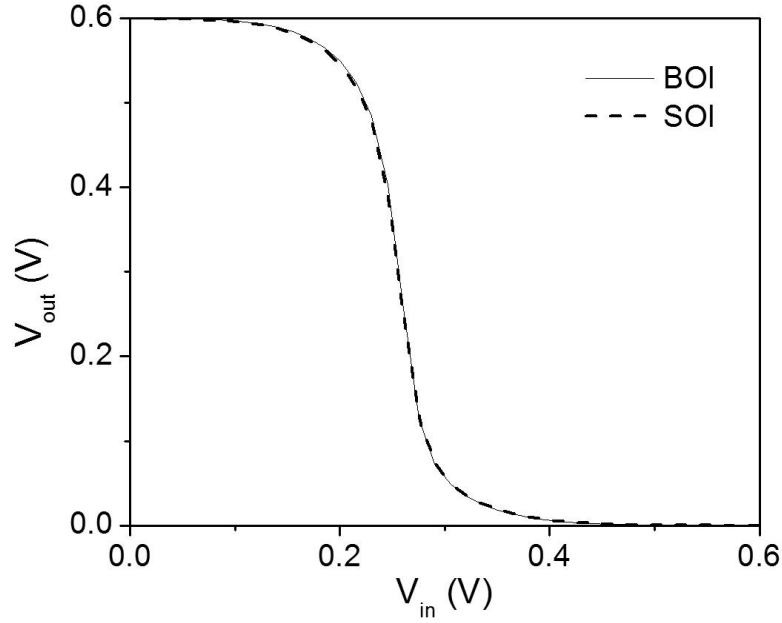
Device	W <sub>fin</sub> (nm)	Workfunction (eV)	DIBL (mV/V)	SS (mV)
<b>n-type BOI</b>	15	4.45	87	79.5
<b>p-type BOI</b>	15	4.45	75	-74.4
<b>n-type SOI</b>	15	4.8	68	74.7
<b>p-type SOI</b>	15	4.8	80	-75.4

To analyze multi-device and circuit performance, we use the TCAD mixed-mode environment for simulation and evaluation of the CMOS inverter logic gate consisting of two different FinFET structure.

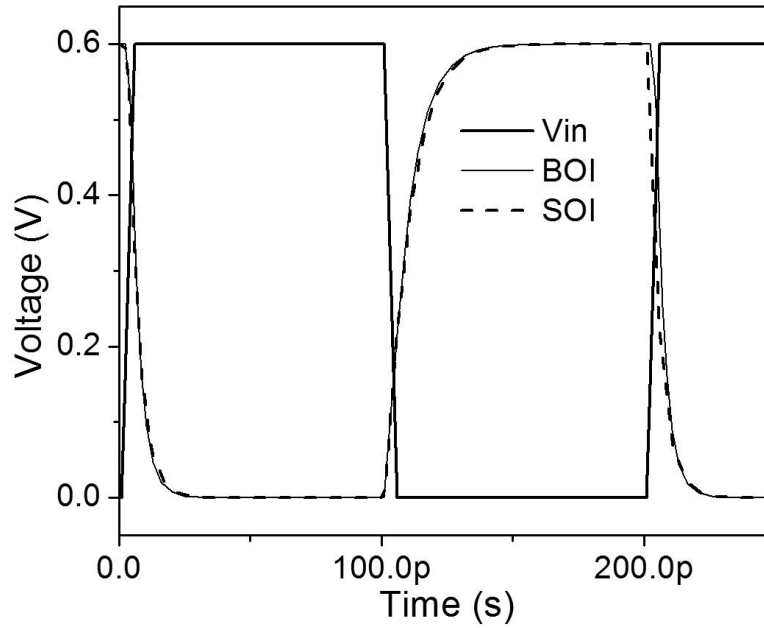
The CMOS inverter Voltage Transfer Characteristics (VTC) in Figure 3.3 shows both BOI and SOI FinFET CMOS inverters have a steep transition region. In addition, the transient simulation results in Figure 3.4 demonstrate its high speed operation capabilities.



**Figure 3.2: Device output device characteristics with SHE of SOI and BOI FinFETs**



**Figure 3.3: Sharp transition is observed from voltage transfer characteristics for both SOI and BOI FinFET based CMOS inverters**

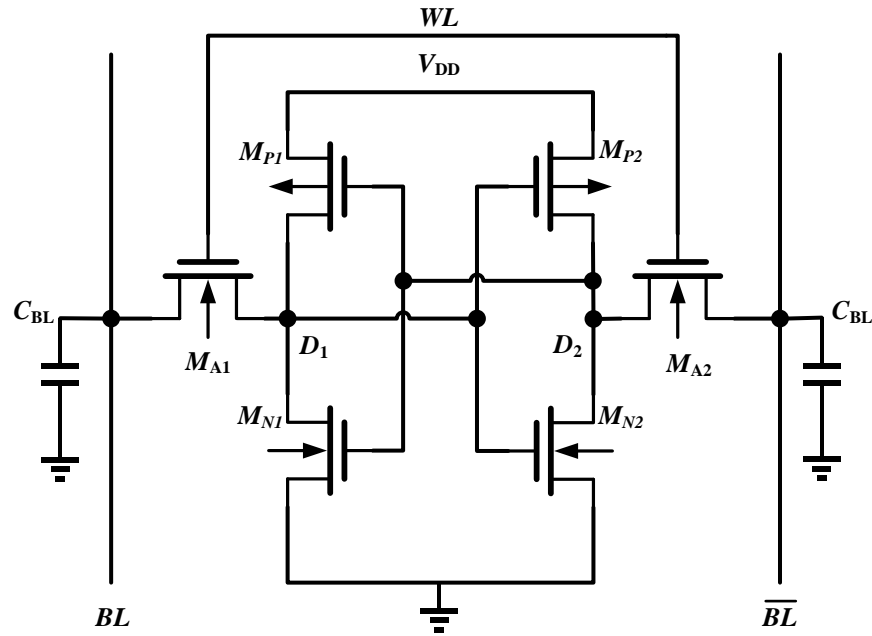


**Figure 3.4: Transient response of both SOI and BOI FinFET based CMOS inverters with a 5 GHz signal input**

### 3.2.2 FinFET Based SRAM Module

A typical SRAM cell uses six MOSFETs to store each memory bit as shown in Figure 3.5. Two additional access transistors connected to the Word Lines (WL) and the Bit

Lines (BL) serve to isolate the latch from other memory cells, and control the access to a storage cell during read and write operations. Each inverter of the latch requires two transistors in NMOS or PMOS technology. The storage cell structure has two stable states which are used to denote 0 and 1. At 0 in the memory cell will correspond to a low voltage level (0 V) on the left-hand data storage node (D1) and a high voltage level ( $V_{DD}$ ) on the right-hand data node (D2); a 1 in the memory cell will correspond to an opposite voltage level assignment.



**Figure 3.5: Schematic of six-transistor SRAM Cell**

An SRAM cell has three different modes: standby mode where the circuit is idle, reading mode when the data has been requested and writing mode when updating the digital information. In standby mode, the access transistors are turned off. The two cross coupled inverters will continue to reinforce each other as long as they are connected to the supply source. In reading mode, once BL voltages have been precharged to the desired level, which is determined by the sense amplifier, cell data can be reached by raising WLs to enable both the access transistors. The next step is that the states stored in

D1 and D2 are transferred to the bit lines by charging or discharging through involved transistors in the latch. For the write mode, BLs are initialized with the corresponding voltage that is to be written into the cell. When the WL is turned on, D1 and D2 will be forced to the logic level connected to the access transistor. Positive feedback will drive the latch into steady state [61].

When evaluating SRAM, we look into the metrics including hold margin, read margin and write time. Hold margin measures the information retention capability of the SRAM. Although it is least sensitive to the noise fluctuation, it is now becoming more of a concern because of the serious gate leakage current and  $I_{on}/I_{off}$  ratio degradation in the shrinking module [62]. To quantify the hold stability, the Hold SNM (static noise margin) is extracted when the SRAM is in the standby mode. The SNM of an SRAM cell represents the minimum DC-voltage disturbance necessary to upset the cell state, and its value is defined as the edge length of the largest square nesting inside the lobes of the butterfly plot formed by the transfer characteristics of the cross-coupled inverters [63]. Similarly, Read stability can be characterized by the read SNM. The Read SNM is defined as the side length of the maximum square that can fit inside the corresponding butterfly curve formed by the voltage transfer characteristics of each inverter when the SRAM is in the read mode [63, 64]. For the Write operation, we use write time to describe the AC performance of the SRAM cell. The Write time of the memory module is defined as “the time it takes for the voltages of two cell storage nodes to cross over after the word-line turns on” [65].

Besides the abovementioned considerations during the design, the need of Low Standby power (LSTP) SRAM also urges the low leakage current, small supply voltage

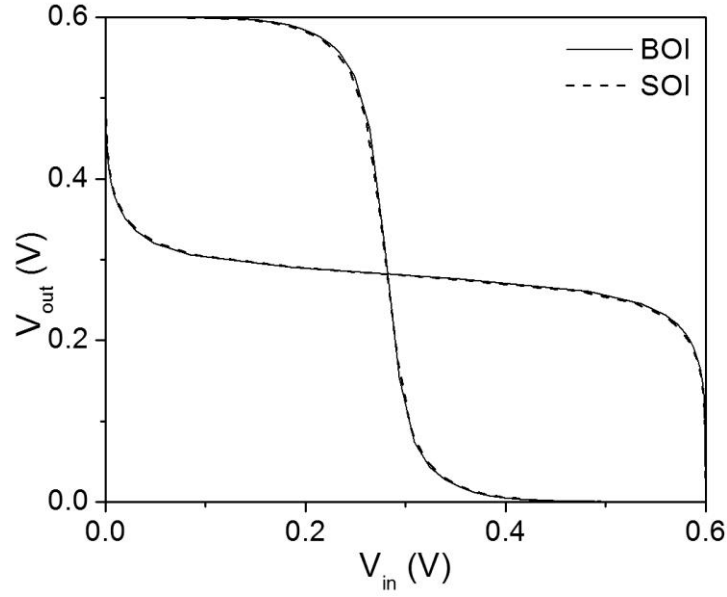
and good subthreshold slope for the transistor unit [2]. For conventional planar SRAM cell, to suppress leakage current, high bulk doping is required in the bulk of the MOSFET transistor. However, high doping will introduce threshold voltage variation which affects the SNM and thereby poses difficulty in the supply voltage scale down [66]. In addition, the reduction of the gate length in planar MOSFET degrades the subthreshold swing and challenges the achievement of small threshold voltage which is desirable for LSTP application [67].

FinFET structure is the promising solution to overcome those barriers and realization of aggressive scaling, economic fabrication, low power consumption, high density integration, and high speed. The enhanced gate control improves channel effect and makes small threshold voltage feasible. Furthermore, a smaller output conductance and reduced DIBL effect help narrow the transition region of the VTC of the inverter and therefore permit large SNM compared to the same node planar MOSFET. Last but not the least, with the space efficiency, FinFET can achieve larger channel width than the planar for high drive current, which can speed up the SRAM operations.

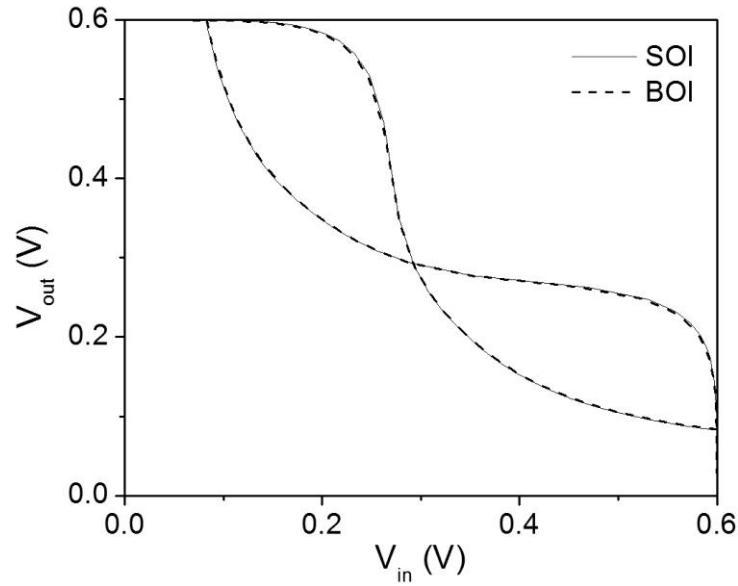
Similarly, we use TCAD mixed-mode simulation method to virtually connect the coupling inverters, provide 0.6 V voltage bias and assign signals to the latch for circuit operation. For FinFET SRAM cell simulation, the hold butterfly which is least sensitive to noise fluctuations and the read one which is most sensitive are extracted. The hold SNMs in Figure 3.6 are 211 mV and 209 mV, whereas the read SNMs in Figure 3.7 are 120 mV and 118 mV, for BOI and SOI based SRAM respectively. SOI based Cell write-1-operation and write-0-operation time are 11.4% and 152% faster than the BOI one as shown in Figure 3.8 since SOI has a smaller parasitic capacitance. Extensive simulation



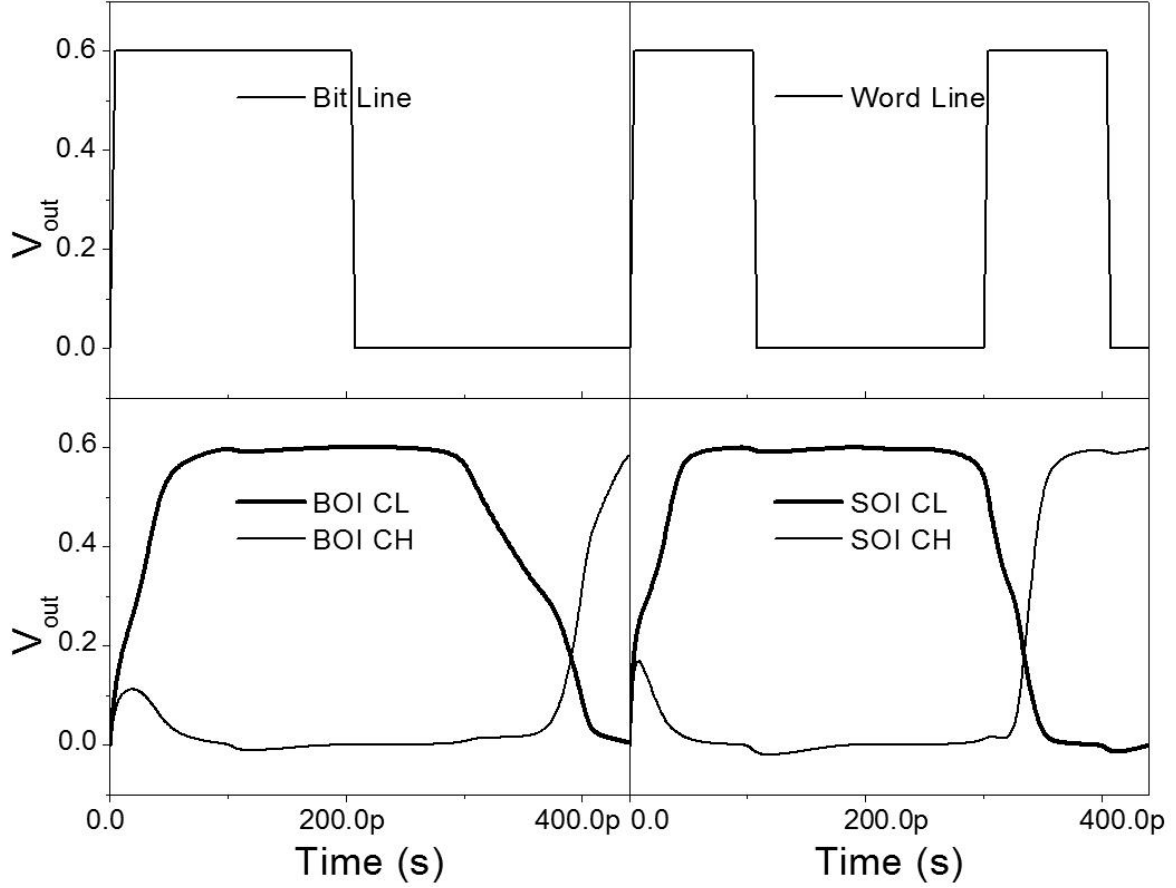
results show that with low operation voltage, BOI and SOI based digital circuits have very similar characteristics. Also, SHE does not degrade circuit performance during low voltage operation.



**Figure 3.6: SRAM Hold butterfly characteristics for both SOI and BOI FinFET based memory modules**



**Figure 3.7: SRAM read butterfly characteristics SOI and BOI FinFET based memory modules**



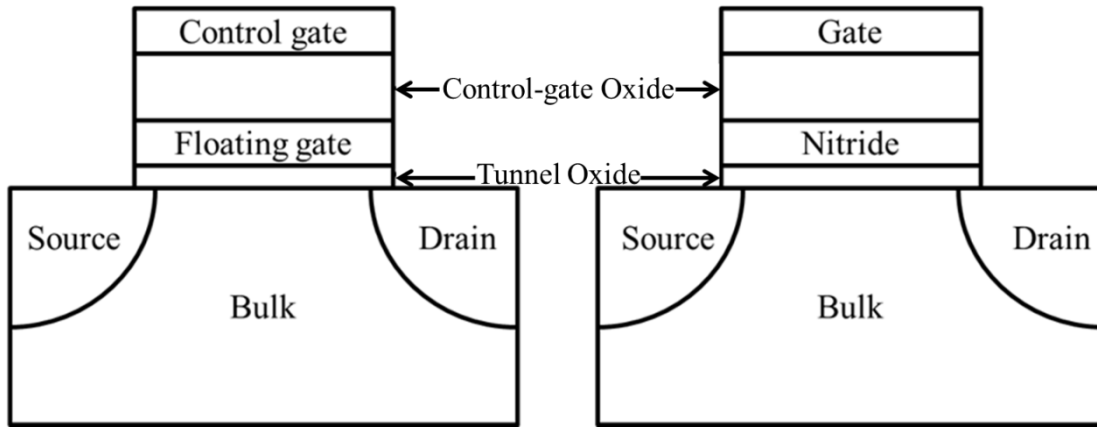
**Figure 3.8: Transient analysis of SRAM cells with a 3.3 GHz word line signal**

### 3.3 FinFET NVM Cell

#### 3.3.1 NVM Cell Operation Mechanism

Different from SRAM memory module, non-volatile memory cell requires only one transistor for bit information storage. The standard flash NVM cell structure is similar to the conventional MOSFET structure, except that its gate and gate oxide are essentially modified. Based on different modification, there are two groups of nonvolatile memory devices: the floating-gate devices and the charge-trapping devices, such as SONOS (Silicon-Oxide-Nitride-Oxide-Silicon) [68]. The latter one has better scalability and short channel effect immunity than the former one especially in sub-50-nm regime due to its

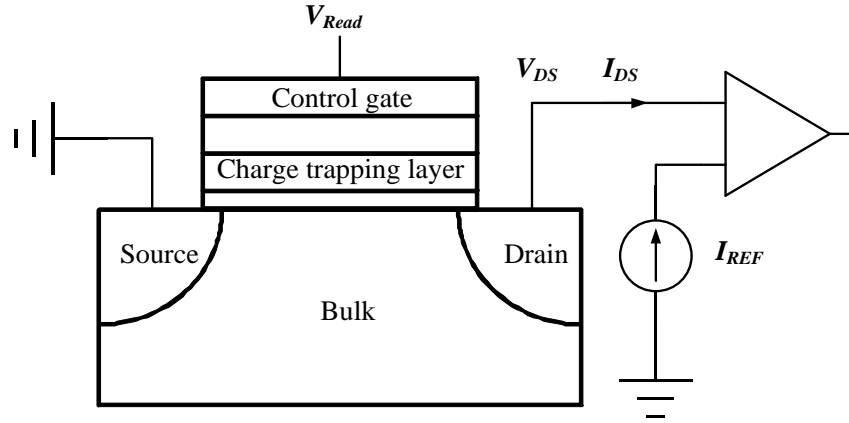
thinner gate-stack equivalent gate oxide thickness [69, 70]. Both device structures are shown in Figure 3.9. Bit information is stored in the floating gate or at the nitride-oxide interface by injected charge across the tunnel oxide. Those stored charges modulate the threshold voltage ( $V_T$ ) of the transistor.



**Figure 3.9: The floating-gate device and the charge-trapping devices (SONOS) [68]**

The  $V_T$  modulation results in two binary states: a low-threshold state (binary state “1”), and a high threshold state (binary state “0”). To optimize device performance, the separation between these two states (threshold voltage window) needs to be maximized so that “1” and “0” state can be properly distinguished; additionally, charge leakage from the charge-trapping film or floating gate must be minimized so that the data can be maintained as long as possible.

A Flash NVM cell has two different modes: reading mode and writing mode to access or modify the stored information. The operation for reading mode refers to the current sensing performed on a NVM cell to determine the digital information stored within it. In practice, this is achieved by biasing the NVM cell with a certain gate-to-source voltage and a relatively large drain-to-source voltage. If electrons are stored in the stack, a high threshold state will lead to low drain current; if no electrons are stored, a low threshold state will lead to high drain current. This operation can be explained by Figure 3.10.



**Figure 3.10: Current measurement is used to determine the binary state**

For the writing mode, there are two basic operations: “program” and “erase”. For each operation, two mechanisms can be involved with charge injection across the tunnel oxide during the operation. In the hot-electron injection programming mechanism, both  $V_g$  and  $V_d$  are biased with a large voltage (with  $V_g > V_d$ ), then the laterally accelerated electrons and the induced ions can be injected into the stack since they overcome the barrier of Si/SiO<sub>2</sub> interface [71]. In the Fowler-Nordheim Tunneling programming mechanism, the source and drain are either kept floating or grounded while a large positive gate voltage is applied to the structure. The electric field across the bottom oxide layer is most critical since the current transport in insulators is generally a strong function of the electric field [72]. For the erase mode, similarly, two mechanisms are employed to remove electrons from the stack of the flash memory cell. The band-to-band tunneling-hole injection erasing mechanism is similar to the hot-electron injection programming mechanism. In this method, the drain is biased to a high voltage and the source is grounded to generate hot carriers close to the drain region, the negative biased gate will direct the holes towards the stack and drive the electron towards the drain region. For the Fowler-Nordheim tunneling erasing mechanism, while keeping in the drain and source

grounded, a large negative transverse field is applied across the device by a high negative gate voltage to swipe away the stored electrons in the stack.

### **3.3.2 Simulation of SONOS FinFET NVM Cell**

Since Fowler-Nordheim mechanism requires large gate bias for NVM cell operation, a great number of grid points are necessary to discretize the whole system for device simulation. This number can be tremendous for a 3-D structure simulation because the SONOS stack requires fine mesh at the interfaces. The huge amount of mesh elements greatly affect the simulation efficiency and thereby dramatically increases the simulation time. Besides, the SONOS device is involved with trapping and de-trapping mechanisms and carrier transport in ONO dielectric stack during the operation. The physics behind those behaviors are still not fully understood [2]. Therefore, the TCAD modeling of such physical phenomena still need significant improvement. Under these conditions, the combination of the large number of mesh elements and preliminary TCAD trapping model seriously challenges the simulation robustness.

To demonstrate the function, scalability and superior device performance of SONOS NVM cell with FinFET structure, we have simulated double gate FinFET structure with ONO gate dielectric in 2-D dimension and applied the Fowler-Nordheim mechanism to illustrate programming and erasing operation of a NVM cell.

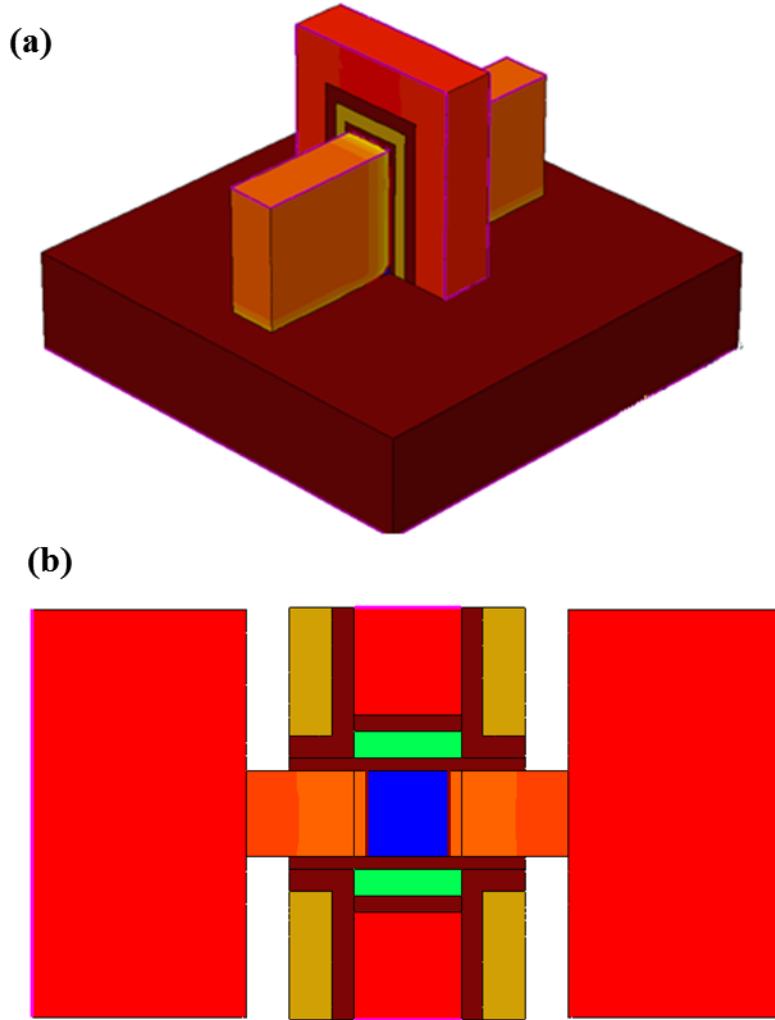
The simulated 2-D architecture can be treated as a cross sectional region taken from the double gate SONOS FinFET standing on a SOI structure as shown in Figure 3.11, where the tunneling gate oxide at the top is thick enough to block the electron invasion. This 22 nm node 2-D structure is designed with a 25 nm gate length and 20 nm fin thickness. For the ONO stack, research reports show that the thickness of the tunnel oxide

layer and control-gate oxide layer should compromise carrier tunneling and retention [73]. Therefore, the thickness of the tunnel oxide layer should be moderate, and the control-gate oxide should be more than 1.5 times thicker than the tunnel oxide to prevent the leakage current toward gate electrode [74, 75]. Therefore, for a 25 nm gate SONOS FinFET, tunnel oxide should be around 3 nm according to the scale down method, the nitride layer will be around 5 nm and the control-gate oxide around 5 nm [69, 76, 77]. Based on above guidelines and extensive TCAD design of experiments, we set up the stack with  $t_{\text{tunnel}} = 3$  nm,  $t_{\text{nitride}} = 6$  nm and  $t_{\text{gate}} = 4$  nm. For the source and drain region, raised source/drain structure (not shown in Figure 3.11 (a) but in Figure 3.11 (b)) is adopted to reduce the parasitic resistance to enhance the number of carriers travelling along the channel and increase the probability of tunneling at the interfaces.

Heavy doping is applied to the source and drain region by constant doping profile definition with the concentration of  $10^{20} \text{ cm}^{-3}$ . Gaussian function is used for gate extension region doping profile definition to mimic the gate doping overlap by the dopant lateral diffusion.

The 2-D structure is meshed with attention paid to the interface to ensure the simulation robustness of tunneling and trapping. The simulation of such a nonvolatile memory is accommodated by velocity-field characteristics, Shockley-Read-Hall Recombination model (a function of doping for generation rate and lifetime of electron-hole-pair), and traps definition. The trap is described by its type, energy and spatial distribution, and capture and emission rate. For the SONOS, we define both the donor trap and the acceptor trap uniformly inside the nitride layer at the concentration of  $10^{19} \text{ cm}^{-3}$  and assign those traps with corresponding energy distribution. Poole-Frenkel model

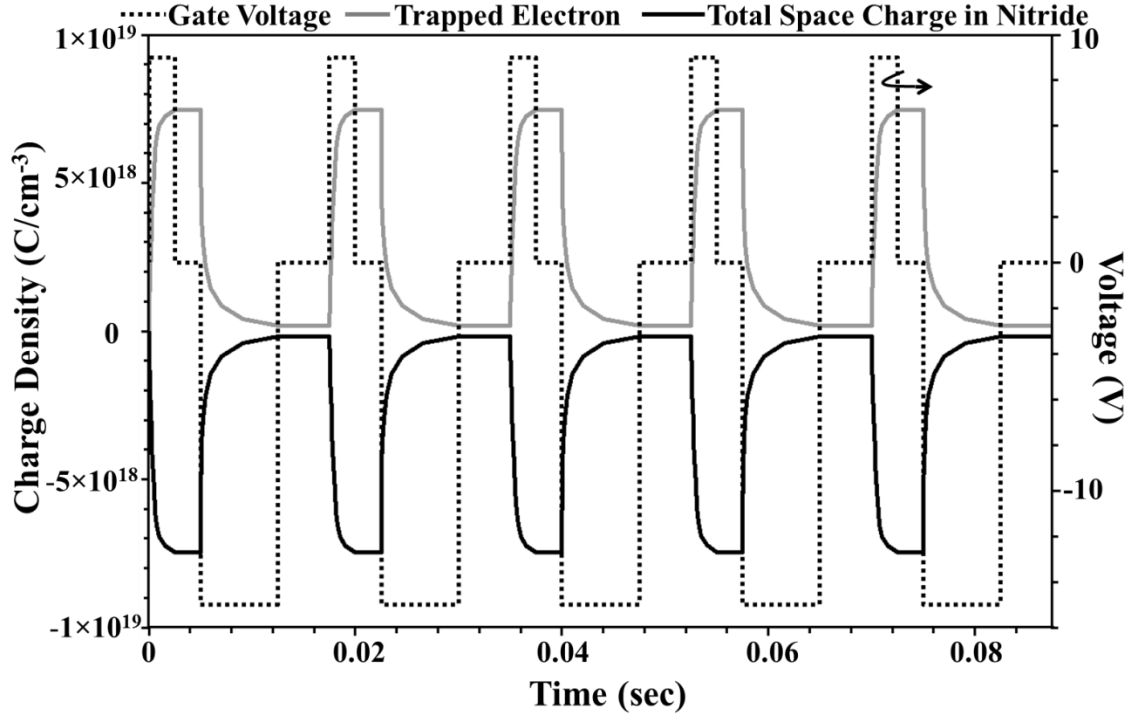
is adopted to interpret transport effects in dielectrics for the prediction of the emission probability for charged trap centers, and the trap capture is specified by carrier barrier tunneling models [32].



**Figure 3.11: (a) 2-D and (b) 3-D structure of a 22 nm node SONOS FinFET**

For the simulation of the SONOS device, we program the device and erase the trapped electrons in the nitride layer for five continuous cycles (see Figure 3.12) to ensure the stable operation (electron trapping and de-trapping) of the memory cell samples virtually fabricated by the DoE. The program operation is executed by a positive enough gate voltage while the erase step is implemented with a larger negative bias. For

these 22 nm node samples, a 9 V gate voltage is applied for 2.5 ms for programming and a -15 V bias is inserted for 7.5 ms for erase operation.

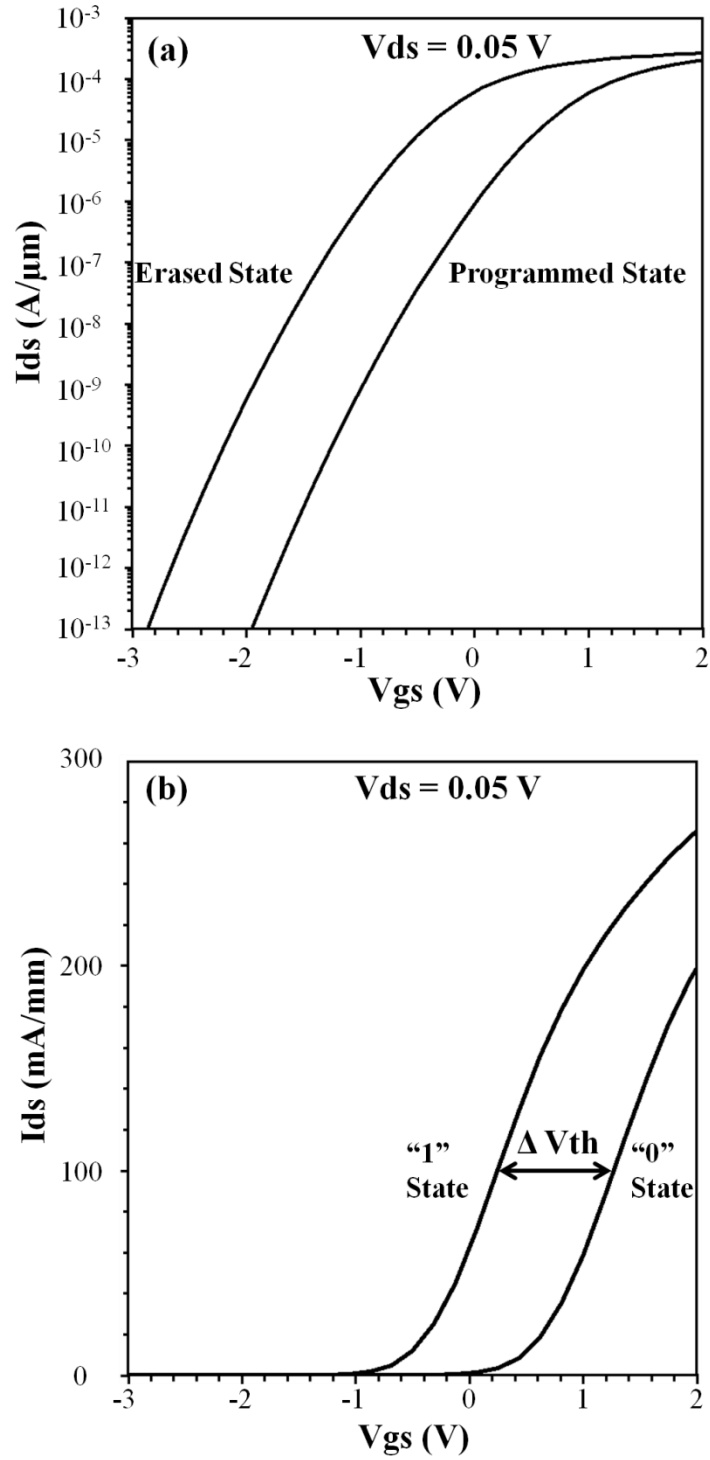


**Figure 3.12: Trapped electron charge and total space charge in nitride region of SONOS device as a function of time during operation cycles**

After the examination of previous simulation results, only steady-state samples are selected towards the extraction of threshold voltage. The saved final programmed and erased states of those devices are then used in the read cycle where an input transfer curve will be plotted.

As shown in Figure 3.12 (a), the programmed state shows an extrapolated threshold voltage of 0.520 V, corresponding to a “0” state whereas the erased state gives an extrapolated one of -0.537 V, corresponding to a “1” state. The resulting threshold voltage window width is 1.057 V. The threshold voltage window feature allows a very small read voltage (around 0.1 V) differentiate two binary states of the NVM cell by sensing the drain current.





**Figure 3.13: (a) Linear scale and (b) logarithmic scale of SONOS FinFET input characteristics for programmed state and erased states**

The logarithmic scale of the input characteristic in Figure 3.13 (b) shows a suppressed leakage current benefiting from the double gate structure. The normalized leakage current

is below 1 pA/ $\mu\text{m}$  and the  $I_{\text{on}}/I_{\text{off}}$  ratio is of the order of magnitude of  $10^{14}$ . Despite the small leakage current, it should be noted that the subthreshold swing is more than 300 mV/dec. This is due to the large value of EOT of the ONO stack, which is required for the proper operation of the SONOS memory cell.

### 3.4 Summary

In this chapter, we have conducted extensive device simulations on FinFET-based digital circuits and memory cells. On one hand, we demonstrate a 22-nm non-volatile SONOS memory cell with small leakage current, small threshold voltage and relatively large threshold voltage window, which make itself suitable for low voltage operation. On the other hand, we compare SOI and BOI FinFETs and volatile memory module designed with those devices. We find out for low voltage supply SHE impact is modest for both devices and circuit performance. SOI FinFET CMOS inverter and SRAM cell characteristics are very close to BOI ones. Therefore, considering the lesser fabrication complexity, SOI FinFET would be more preferable than BOI FinFET for the design of low power digital circuits.

# Chapter 4

## Optimization of Multi-Fin FETs for RF/Analog Applications

### 4.1 Introduction

The steady improvement in the digital performance of the silicon device pushed by Moore's Law also leads to the advancement of radio frequency and mixed-signal (RFAMS) technologies [2]. As the semiconductor market rapidly diversified, RFAMS technologies became essential and critical to meet the increasing demand in wireless communication. However, it is noted that some of the techniques such as dimensional structural changes and material engineering deployed in the digital roadmap have somehow harmed or at least altered transistor RF and analog metrics. As Moore's Law stepped into the sub 32 nm node, tradeoffs in device design and optimization need further investigation. As discussed in the previous chapters, the introduction of the 3-D fin body fundamentally changes the dimensional structure of the MOSFET. The enhanced gate controllability of FinFET eliminates the need for high doping in the bulk and therefore the implementation of the intrinsic undoped silicon body becomes feasible. However, the design and control of doping in the neighborhood of the gate edge are important technological challenges in the optimization of the device characteristics, especially for RF/analog figure of merits [78].

The RF/analog figure of merits (FOMs) refer to device characteristics such as the cut-off frequency  $f_t$ , the maximum oscillation frequency  $f_{\max}$ , the intrinsic gain  $A_{vo}$ , the

transconductance  $g_m$ , the noise figure performance, the mismatch behavior, etc. These metrics are closely associated with device intrinsic and extrinsic parasitic components [79]. The intrinsic parasitic components are the inner parasitic resistance such as Ohmic contact resistance, gate-to-source/drain resistance, and inner parasitic capacitance such as gate capacitance and gate-to-source capacitance. The extrinsic parasitic components are related to the pad, the interconnect parasitics and the coupling among them and the devices.

We have discussed the aspect ratio optimization of the single fin device with raised source/drain structure in Chapter 2 for the short channel effects management. Besides the dimensional design parameters of the device, the doping profile discussed in this chapter influences device electrical characteristics as well. For instance, the lateral movement of the dopants determines the source and drain overlap or underlap condition, to alter the effective channel length and thereby the parasitic resistance and capacitance. In other words, a lateral diffusion of the dopant in the extension region with different junction abruptness and the dopant profile gradient in the source/drain extension region impact on both short channel effects and the parasitic components important for RF/analog FOMs [80]. In addition to the doping distribution analyzed in this chapter, we have also included and modeled the extrinsic components in the device mixed-mode simulation for comprehensive evaluation of multi-fin RF/analog FOMs.

## **4.2 Design and Optimization of Base FinFET Unit**

The doping profile is utilized in source/drain engineering for device characteristics optimization. Generally, there are two kinds of S/D doping approaches: overlap and underlap. Figure 4.1 (a) and (b) illustrate the source and drain underlap and overlap

structure concept. In TCAD design, such a doping profile can be realized by employing analytical equations in the lateral direction to model the dopant distribution in the real device. The lateral equation is defined as Gaussian source/drain profiles function ( $N_{SD} \propto \exp(-y^2/\sigma_{S/D}^2)$ ) with lateral straggle  $\sigma_{S/D}$  which describes the diffusion of the dopants towards the channel as shown in Figure 4.1 (c) [81]. It is noted that the small lateral straggle indicates quick degradation which leads to abrupt junction while the large one indicates slow degradation resulting in a non-abrupt doping profile. The abrupt junction, which rolls off from the gate edge with  $\sigma_{S/D} = 1\text{nm}$ , consists of the boundary of a uniform heavily doped source/drain region (including the extension region) with a slightly source/drain doping profile overlap as illustrated in Figure 4.1 (c). In contrast, the slow rolling-off of the doping concentration starting from the source/drain edge leaves the part of the extension region sharing the same doping type as the fin body and result in a gap between the source/drain region boundary and the gate edge. The dopant lateral diffusion should be precisely controlled to avoid large parasitic resistance of the extension region by a very small  $\sigma_{S/D}$ , and to prevent punchthrough by a very large one.

When evaluating multi-fin FETs device characteristics, we should be aware that RF/analog transistors are typically designed with large total widths to obtain high transconductance, good noise figure and improved mismatch performances [79]. For the multi-fin structure, the extension of the width is achieved with the help of a bunch of fins. Given that base FinFET units within the multi-fin configuration are nominally identical to each other under the same fabrication process, the optimization of the multi-fin FETs device intrinsic characteristics should give full consideration to the base FinFET.

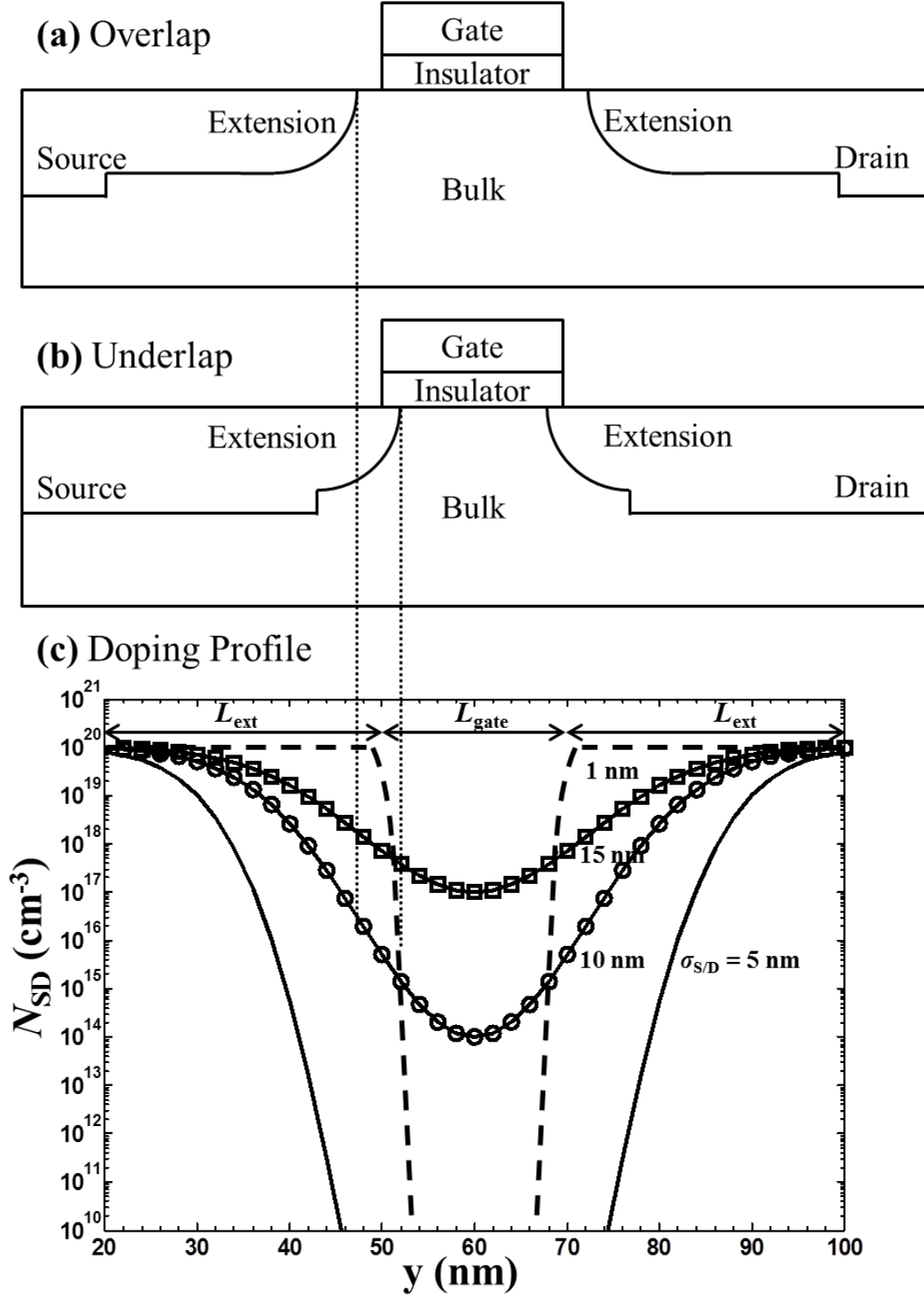


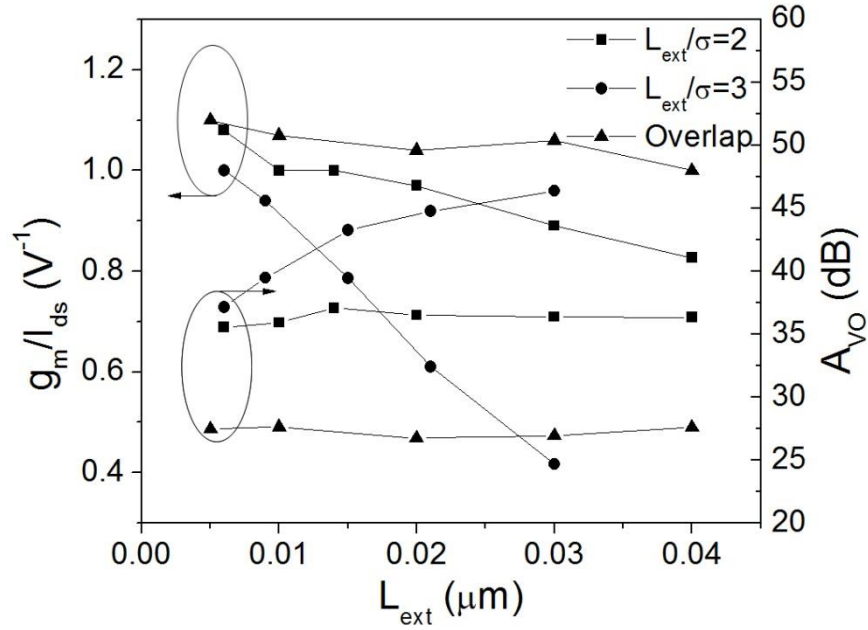
Figure 4.1: (a) Overlap and (b) underlap doping profile with (c) analytical doping function illustration

Therefore, we first optimize analog/RF FOM of a 22 nm node single fin FinFET. The optimized device is then used as a base unit of multi-fin structure. The gate length ( $L_g$ ) of this n-type FinFET is set at 25 nm. The fin height ( $H_{fin}$ ) is fixed at 50 nm. The bulk is lightly doped  $10^{15} \text{ cm}^{-3}$  to avoid the dopant fluctuation. Selective epitaxial growth with heavy doping is performed for the source/drain region to minimize the parasitic resistance. SDE region engineering is considered by the application of overlap and underlap design. Abrupt junction, which is achievable by solid re-growth and laser annealing process [82], is designed with a fast doping decay with lateral straggle ( $\sigma_{S/D}$ ) at the value of 1 nm/dev at the edge of SDE region whereas the underlap doping profile in the SDE region is simulated with a Gaussian model rolling off from a peak value of  $10^{20} \text{ cm}^{-3}$  at the edge of the source/drain. The EOT of the Hf-based dielectric in the simulation is 0.7 nm. The work-function of the TiN metal gate is adjusted to 4.6 eV such that the threshold voltage  $V_t$  of the device is around 0.3 V. The device is investigated with a calibrated TCAD simulation taking into account quantum effect with Lombardi mobility model [32].

The design of TCAD experiments for simulation is shown in Table 4.1. For this study, we have considered the trade-off between current drivability and SCEs. Results show that overlap design enhances current drive at the cost of SCEs due to the S/D encroachment into the channel. Thin  $W_{fin}$  can alleviate the SCEs but it degrades the drive current since the SDE resistance is larger. Underlap design specified by spacer length to lateral doping gradient ratio ( $L_{ext}/\sigma_{S/D}$ ) keeps a good compromise between the drain current and SCEs, and shows great potential in SDE region engineering [80-82]. It shows a larger intrinsic gain ( $A_{VO}$ ) than overlap one and a comparable  $g_m/I_{ds}$  ratio when  $L_{ext}/\sigma_{S/D} = 2$  (See Figure 4.2).

**Table 4.1: TCAD-predicted SCEs of the 22-nm node DG nFinFET at room temperature for SDE engineering**

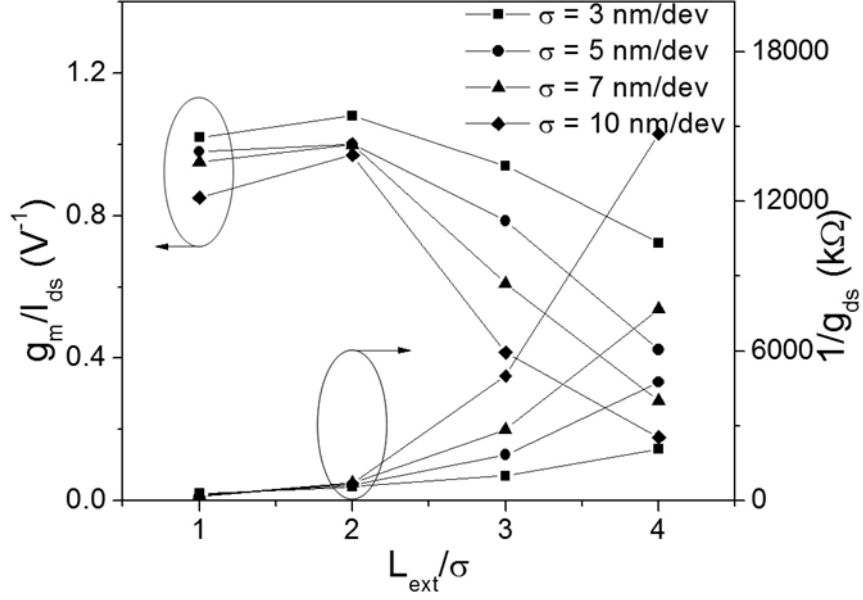
$W_{\text{fin}}$ (nm)	$L_{\text{ext}}$ (nm)	$\sigma_{\text{S/D}}$ / (nm/dec)	DIBL (mV/V)	S (mV)	$I_{\text{off}}$ (A/ $\mu\text{m}$ )	$I_{\text{on}}$ (A/ $\mu\text{m}$ )
17	10	Overlap	146	101.2	6.2e-7	1.2e-3
17	10	5	85	76.1	3.9e-10	9.1e-4
17	20	Overlap	154	99.4	7.8e-7	1.2e-3
17	20	10	72	74.3	2.0e-9	7.6e-4
12	10	Overlap	73	77.9	2.6e-9	1.1e-3
12	10	5	34	66.2	6.9e-11	8.4e-4
12	20	Overlap	77	76.4	3.2e-9	1.0e-3
12	20	10	29	65.6	4.4e-11	6.7e-4



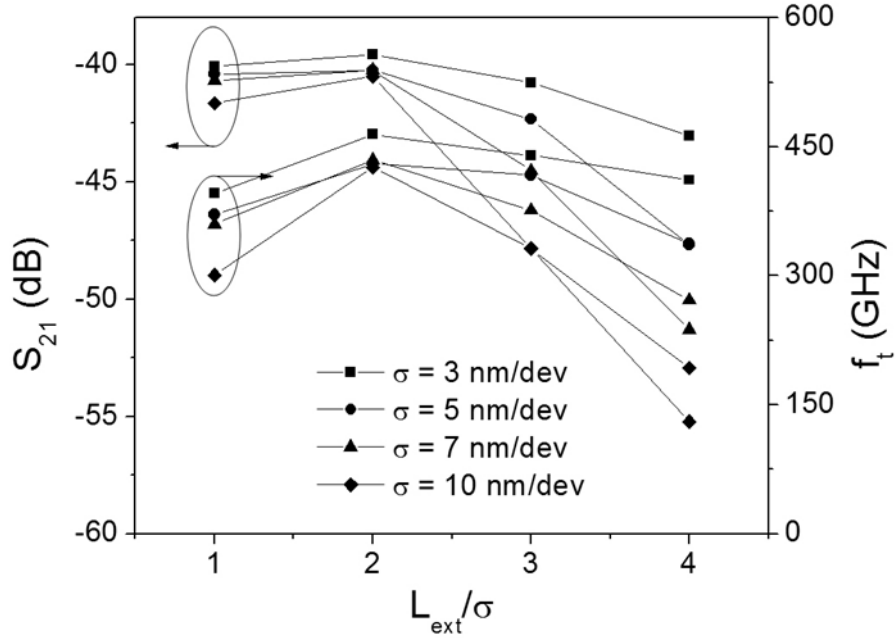
**Figure 4.2: Variation of  $g_m/I_{\text{ds}}$  and  $A_{\text{Vo}}$  versus  $L_{\text{ext}}$ . Device parameters:  $W_{\text{fin}} = 12$  nm, and  $V_{\text{ds}} = 1.0$  V.**

Simulation results indicate that as  $L_{\text{ext}}/\sigma_{\text{S/D}}$  goes beyond 2 and  $L_{\text{ext}}$  increases,  $A_{\text{Vo}}$  rises but  $g_m/I_{\text{ds}}$  decreases quickly. The degradation is also demonstrated in Figure 4.3, where a longer  $L_{\text{ext}}$  and a larger  $\sigma_{\text{S/D}}$  bring about a poorer  $g_m/I_{\text{ds}}$  ratio for different  $\sigma_{\text{S/D}}$  devices with a fixed  $L_{\text{ext}}/\sigma_{\text{S/D}}$ . These degradations are due to increase of the undoped portion in SDE region that extends the effective channel length [81], indicating an increase of  $1/g_{\text{ds}}$  as demonstrated in the same figure.





**Figure 4.3: Variation of  $g_m/I_{ds}$  and  $1/g_{ds}$  for various  $\sigma_{S/D}$  value. Device parameters:  $W_{fin} = 12$  nm, and  $V_{ds} = 1.0$  V.**



**Figure 4.4: Variation of  $S_{21}$  and  $f_T$  versus  $L_{ext}/\sigma_{S/D}$  ratio extracted at  $I_{ds} = 100$   $\mu A/\mu m$  for various  $\sigma_{S/D}$  value. Device parameters:  $W_{fin} = 12$  nm, and  $V_{ds} = 1.0$  V.**

Figure 4.4 shows the analog/RF FOM extracted at the current level of 100  $\mu A/\mu m$ . Both the available  $S_{21}$  (at 10 GHz) and intrinsic cut off frequency ( $f_T$ ) reach maximum when  $L_{ext}/\sigma_{SD} = 2$ . Considering the fabrication fluctuation and compromise among  $g_m$ ,  $A_{vo}$ ,

$f_T$  and SCEs, the optimal value of  $L_{\text{ext}}/\sigma_{\text{SD}}$  ratio for the base FinFET will be 2 with a 20 nm spacer length.

### 4.3 Design and Evaluation of Multi-Fin FETs

For a single fin FinFET, boosting of  $g_m$  to meet the gain requirement of RF applications happens at the cost of SCEs and with a tall  $H_{\text{fin}}$ , which also brings difficulties in manufacturing process. Alternatively, the multi-fin configuration constructed with a number of fingers ( $N_{\text{finger}}$ ) and multiple fins per fingers ( $N_{\text{fin}}$ ) shows a practical means to ease those concerns. The total number ( $N_{\text{finfet}}=N_{\text{finger}}\times N_{\text{fin}}$ ) of FinFETs in such a structure usually is large, i.e., several hundreds of transistors [79]. Considering the complexity and realistic time limit of the simulation in TCAD, we have simplified the structure in Ref. [79] by setting  $N_{\text{finger}} = 1$  as shown in Figure 4.5. The spacing between each fin is set as 50 nm to suit the 22 nm node technology and to achieve optimum RF characteristics [78].

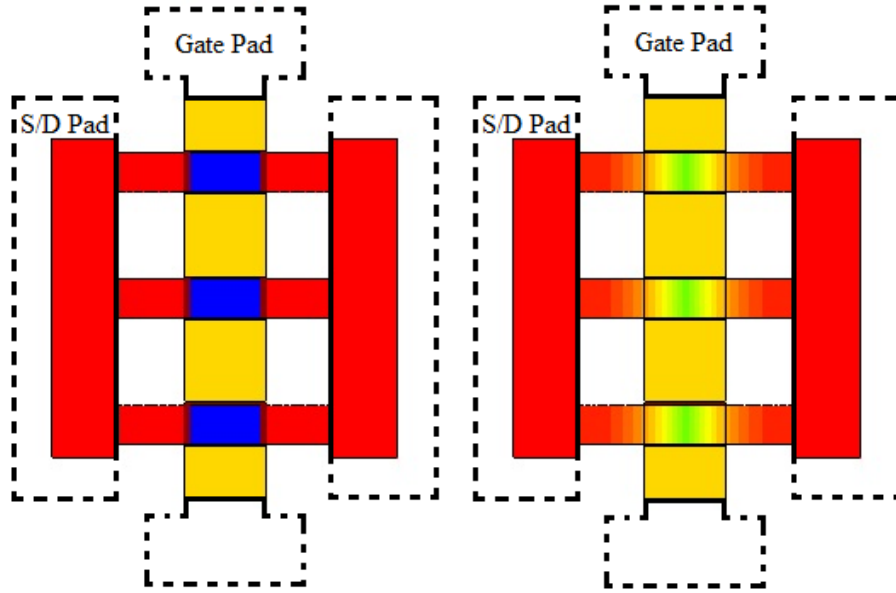
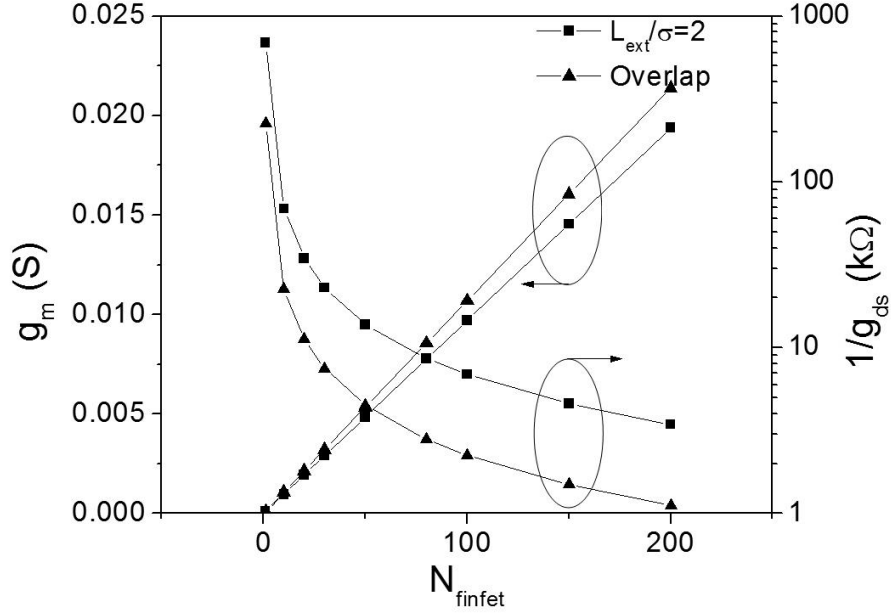


Figure 4.5: Schematic diagram of overlap and underlap multi-fin structure

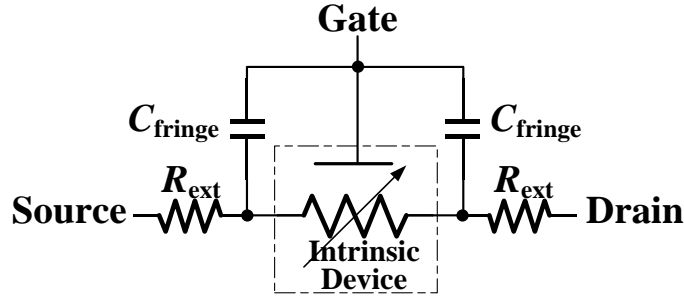
Simulation results in Figure 4.6 show a good linearity between the intrinsic  $g_m$  and  $N_{\text{finfet}}$  for both underlap and overlap design models. It should be noted that the intrinsic  $A_{\text{vo}}$  for multi-fin FETs does not benefit from the arrays of transistors. It is limited to the base unit analog FOM because of the following relation  $A_{\text{vo}} = N_{\text{finfet}} g_m / N_{\text{finfet}} g_{\text{ds}} = g_m / g_{\text{ds}}$ . This relationship is verified and shows the degradation of  $1/g_{\text{ds}}$ , as expected in Figure 4.6.



**Figure 4.6:** Variation of  $g_m$  and  $1/g_{\text{ds}}$  extracted at  $I_{\text{ds}} = 100 \mu\text{A}/\mu\text{m}$  as a function of  $N_{\text{finfet}}$  at 10 Hz. Device parameters:  $W_{\text{fin}} = 12 \text{ nm}$ , and  $V_{\text{ds}} = 1.0 \text{ V}$ .

The RF figure of merits  $f_t$  and  $f_{\text{max}}$  are simulated using the TCAD mixed-mode module with the consideration of the parasitic resistance and the capacitance associated with gate pad, S/D contact and coupling effects. Those extrinsic components are identified as the bottleneck of the RF performance and the values depend on process techniques. A simple model of the base FinFET along with extrinsic parasitic components is shown in Figure 4.7. In the simulated multi-fin structure, the parasitic gate capacitance is mainly due to the fringe capacitance  $C_f$  which is set at  $0.18 \text{ fF}/\mu\text{m}$  for a base FinFET as per ITRS [2]. For the multi-fin structure,  $C_{\text{fmulti}}$  is almost linearly proportional to  $N_{\text{finfet}}$

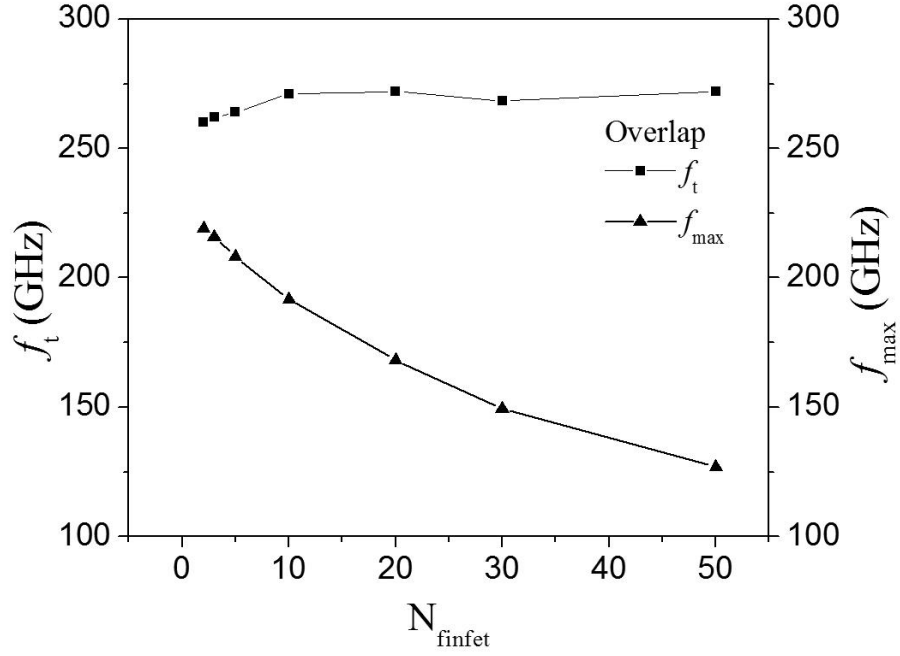
[79] and therefore we can conclude that  $C_{\text{fmulti}} = N_{\text{finfet}} C_f$  for simulation simplification purpose. According to ITRS, the value of contact-area-dependent series  $R_{\text{sd}}$  is  $250 \Omega \cdot \mu\text{m}$ . For a single fin, the contact area of the S/D pad is designed as  $0.04 \times 0.06 \mu\text{m}^2$ . As the fin number increased, the spacing between each fin will be covered with contact and we model  $R_{\text{sdmulti}} = R_{\text{sd}} \times [6/(7 N_{\text{finfet}} - 1)]$ . For parasitic gate resistance, the value of a single fin is set as four times as the  $R_{\text{sd}}$ , due to the limited contact area, to be  $1000 \Omega \cdot \mu\text{m}$ , including a  $50 \Omega \cdot \mu\text{m}$  for the gate pad component. Therefore, for multi-fin,  $R_{\text{gmulti}} = 50 + 950/N_{\text{finfet}}$ . Including the parasitic components, the simulated RF FOM is shown in Figure 4.8 and Figure 4.9.



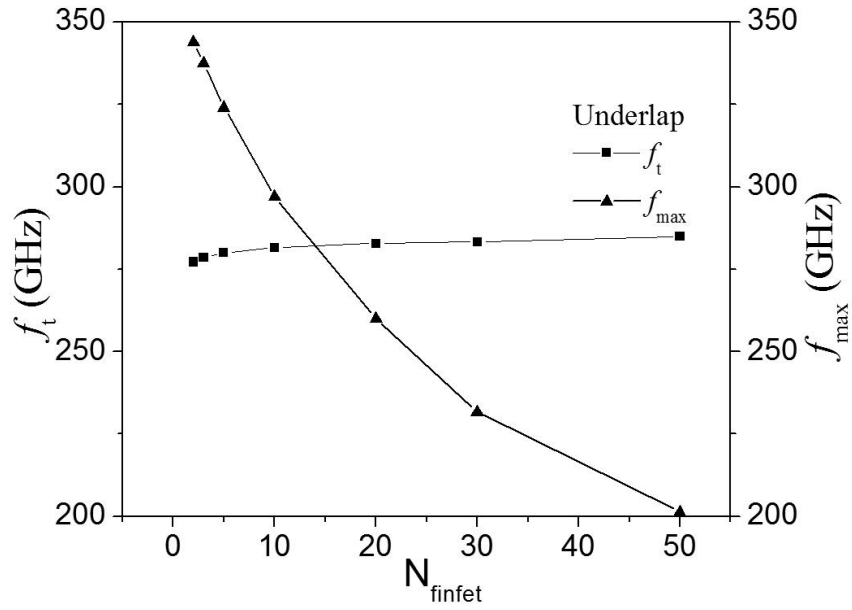
**Figure 4.7: A simple model of base FinFET unit along with extrinsic parasitic resistance  $R_{\text{ext}}$  and fringe capacitance  $C_{\text{fringe}}$  [83]**

For  $N_{\text{finfet}} = 2$ , the overlap structure shows  $f_t$  of 260 GHz and  $f_{\text{max}}$  of 219 GHz, which is consistent with the reported result [78]. As  $N_{\text{finfet}}$  increases,  $f_t$  does not vary a lot according to the equation that  $f_t \approx g_m/[2\pi \cdot (C_{\text{ggintrinsic}} + C_f)]$ , where transconductance and the capacitances share the same factor  $N_{\text{finfet}}$ . However,  $f_{\text{max}}$  starts to degrade because the large component  $R_{\text{gmulti}}$  is non-linearly inversely proportional to  $N_{\text{finfet}}$  and this leads to the decrease of  $f_{\text{max}}$  based on the equation in Ref. [84]. The smaller  $f_{\text{max}}$  for overlap multi-fin structure limits its RF application especially when  $N_{\text{finfet}}$  reaches 10. In contrast, the underlap design, shows a comparable  $f_t$  and a much higher  $f_{\text{max}}$ , compared to the corresponding overlap design. The higher  $f_{\text{max}}$  value is due to the significant reduction in

$g_{ds}$  (Figure 4.6) [78]. As  $N_{finfet}$  increases, even though underlap structure shows degradation in  $f_{max}$  as overlap one, it still maintains the maximum frequency and cutoff frequency above 200 GHz even when  $N_{fin}$  reaches 50.



**Figure 4.8:**  $f_t$  and  $f_{max}$  of overlap structure extracted at  $V_{gs} = 0.6$  V. Device parameters:  $W_{fin} = 12$  nm, and  $V_{ds} = 1.0$  V.



**Figure 4.9:**  $f_t$  and  $f_{max}$  of underlap structure extracted at  $V_{gs} = 0.6$  V. Device parameters:  $W_{fin} = 12$  nm, and  $V_{ds} = 1.0$  V.

## 4.4 Summary

In this chapter, with extensive calibrated TCAD simulations, we present results for SCEs and analog/RF FOM of a single FinFET and multi-fin FETs. The effect of SDE engineering on the analog/RF performance of multi-fin device is studied. Simulations along with theoretical analysis establish the realistic application potential of underlap design for multi-Fin FETs' RF operation.

It is shown that the multi-fin FETs will be particularly useful at sub-32 nm regime for the development of devices for RF applications. Even with a large number of  $N_{\text{finfet}}$ , using underlap design in SDE region with an optimal value of  $L_{\text{ext}}/\sigma_{\text{S/D}}$  ratio, good SCE is achieved and its RF FOM  $f_t$  and  $f_{\text{max}}$  are better than the one with overlap design. Furthermore, the cost of multi-fin device is expected to be lower than other heterojunction devices and III-V compound devices because of its compatibility with the CMOS planar process technology.

# Chapter 5

## Design and Simulation of Enhancement-mode N-polar GaN Single-channel and Dual-channel MIS-HEMTs

### 5.1 Introduction

Nitride III-V compounds, such as Gallium Nitride, Aluminum Nitride (AlN) and their ternaries, can be grown in either Wurtzite or Zinc-Blende phase material system. The former crystal system, the most common phase of nitride materials adopted in electronic devices, is a structure of hexagonal lattices where tetrahedrally coordinated Ga (Al) and N atoms present ABABAB stacking as shown in Figure 5.1 [85].

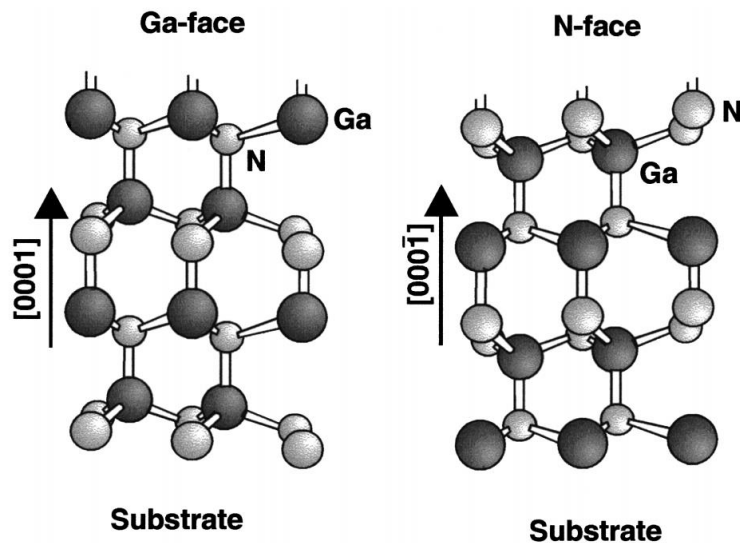
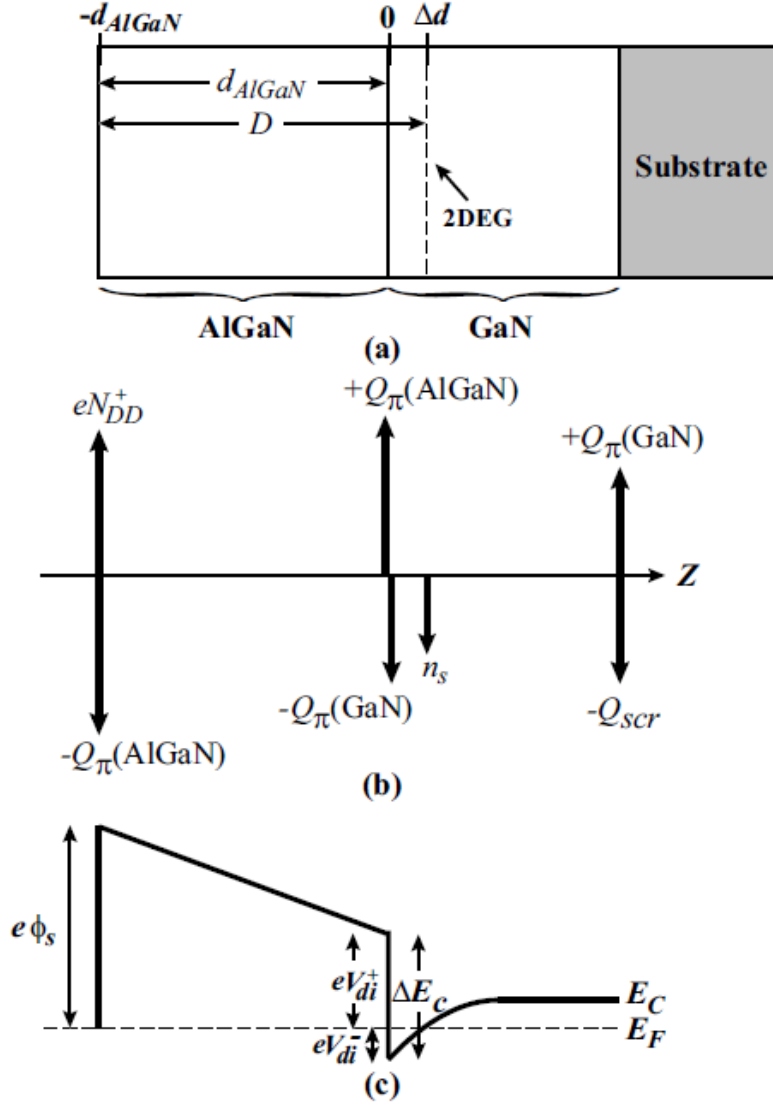


Figure 5.1: Crystal structures of Wurtzite Ga-polar and N-polar GaN [86]

The non-centrosymmetric nature of the Wurtzite structure causes nonzero volume dipole moments in the nitride crystal even when no external strain or electric field applied, leading to spontaneous polarization within the nitride materials. In addition, the piezoelectric property of nitride materials can also develop strain related polarization in the material [87]. In a heterostructure consisting of nitride materials, the net polarization from the spontaneous and the piezoelectric contributions create electric fields within the layers and polar charges at the heterointerfaces [88]. Figure 5.2 illustrates the charge distribution and bandgap diagram of a conventional Ga-polar AlGaN/GaN heterostructure. To maintain charge neutrality, the distributed positive charges at the interface will induce 2-D electron gas (2DEG) channel region where superior mobility can be achieved benefiting from the quantum well confinement and absence of the dopant [88].

GaN HEMTs, taking advantage of spontaneous and piezoelectric polarization, have demonstrated higher power density and higher efficiency than conventional silicon and gallium arsenide based RF and power devices [89-91]. Until recently, improvements in the design of GaN semiconductor device had focused on Ga-polar GaN based HEMTs [92-94]. However, the conventional Ga-polar HEMT usually requires advanced process techniques such as the gate-recess structure, the fluorine plasma treatment or capping layers in making enhancement-mode (E-mode) device. Those approaches can deplete the 2DEG underneath the gate region but suffer from either controllability issue or lattice damage problem [95]. Lately, N-polar GaN, which has a reverse polarization field, shows the advantage over Ga-polar device in making E-mode device with low access resistance, and in particular, for low voltage operation [96-98].





**Figure 5.2: (a) Typical AlGaN/GaN heterostructure along with (b) the charge distribution and (c) the band diagram of the structure [88]**

In N-polar GaN transistor, the natural back barrier, which induces the 2DEG, allows the introduction of capping layer gate dielectric for 2DEG depletion to enable the E-mode operation of the device with a simpler fabrication process, a better threshold voltage control and an improved electron confinement [99]. Besides, the capping mesa can easily include passivation layer or high-k dielectric to suppress current collapse or gate leakage. Moreover, in source and drain access region of N-polar GaN structure, the Al(Ga)N-barrier-free feature permits easier access from contact electrode to 2DEG channel

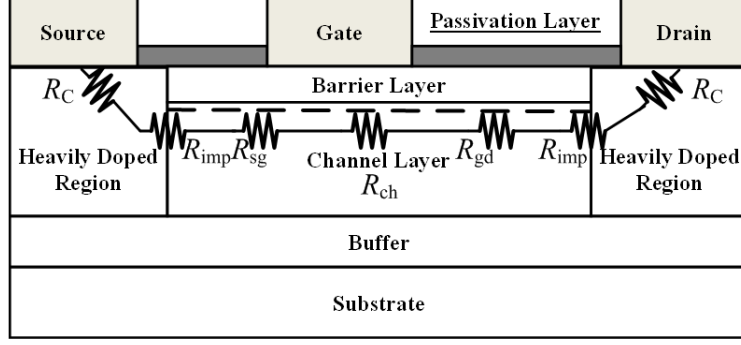
through the regrown n+ GaN region. With the feasibility of non-alloyed Ohmic contacts, the access region resistance can be further reduced for drive current enhancement [100, 101]. Very recently, an E-mode N-polar GaN MISFET device with non-alloyed Ohmic contact was demonstrated to achieve a threshold voltage of 1 V and a high drive current of 0.74 A/mm and small on-resistance of  $2\ \Omega\cdot\text{mm}$  at a gate length of 0.62  $\mu\text{m}$  [97]. N-polar GaN HEMTs also shows competitive breakdown performance and output characteristics to Ga-polar counterparts. A depletion-mode N-polar GaN HEMT on sapphire substrate with 0.8  $\mu\text{m}$  gate drain spacing, showed a breakdown voltage of 170 V and a record power density of 12.1 W/mm under 50 V drain bias at 4 GHz [102].

Despite the increased performance of N-polar devices, we notice that the drive current under low voltage bias for N-polar GaN HEMT is smaller than the state-of-the-art Ga-polar GaN HEMT. In addition, there are even fewer analytical and simulation models developed for E-mode N-polar GaN HEMT. In this chapter, using a 2-D simulation in Synopsys TCAD, N-polar GaN E-mode single-channel MIS-HEMTs are investigated; an E-mode N-polar GaN dual-channel MIS-HEMT is designed and the mechanism of the drive current enhancement is identified; and the impact of GaN layer scaling on device performance is studied.

## **5.2 Design Considerations of GaN HEMT for Low Voltage Operation**

To achieve high current under the low voltage E-mode operation, positive threshold voltage and small on-resistance are expected. The former can be realized by the employment of an N-polar GaN stack as discussed in the previous section. The latter, on-resistance, is an important figure of merit which impacts on drain current as well as the





**Figure 5.4: Regrown S/D region GaN HEMT on-resistance model [103]**

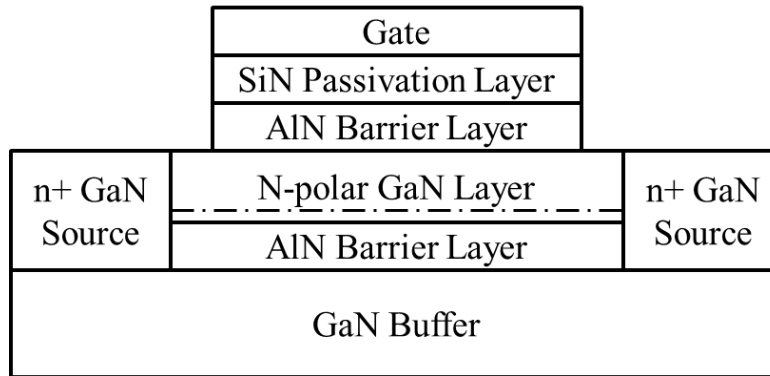
By comparing both on-resistance models,  $R_{on}$  can be divided into  $R_{access}$  and  $R_{sd}$ , where  $R_{access} = R_c + (R_{imp})$  and  $R_{sd} = R_{sg} + R_{ch} + R_{gd}$ .  $R_c$  used to be a large component due to the large Schottky barrier height blocking electron flow. However, with the introduction of the regrown source/drain structure aggressively reducing  $R_c$ ,  $R_{sd}$  becomes an important factor in the determination of the on-resistance. To enhance the drive current of the HEMT, channel resistance reduction should be given full consideration.

### 5.3 E-mode N-polar GaN Single-Channel MIS-HEMT

The E-mode N-polar GaN MIS-HEMT is studied by two dimensional TCAD simulations. The device structure is shown in Figure 5.5. The  $0.62 \mu\text{m}$  gate length transistor comprises an N-polar stack which consists of a 2 nm AlN back barrier, a 20 nm unintentionally GaN layer and a 2 nm AlN capping layer, used as the experimental device structure [97]. The binary material AlN, which has Wurtzite crystal structure as GaN, is believed to lower the on-resistance since it can bring superior electron mobility due to the alloy disorder elimination, and higher 2DEG density due to the larger polarization charge difference with GaN. The AlN/GaN/AlN sandwich structure is being exploited to ensure 2DEG depletion in N-polar GaN layer under zero bias and 2DEG generation as the

positive gate voltage is applied. The mesa is virtually grown on GaN buffer and has a SiN passivation layer, which also functions as a gate dielectric, on top of it.

The source and drain regions are heavily doped with a concentration of  $1 \times 10^{21} \text{ cm}^{-3}$  to mimic regrown n+ access region which can be achieved either by selective silicon implantation or by source/drain molecular beam epitaxy (MBE) regrowth technology. Non-alloyed Ohmic contacts made on heavily doped source/drain region further reduce the access region resistance from the contact electrode to the active region. A  $0.027 \text{ } \Omega \cdot \text{mm}$  contact resistance is reported for such Ohmic contacts of an experimental N-polar GaN device [97]. Accordingly, we assume perfect electrode contact condition in the simulation for improved convergence purpose.

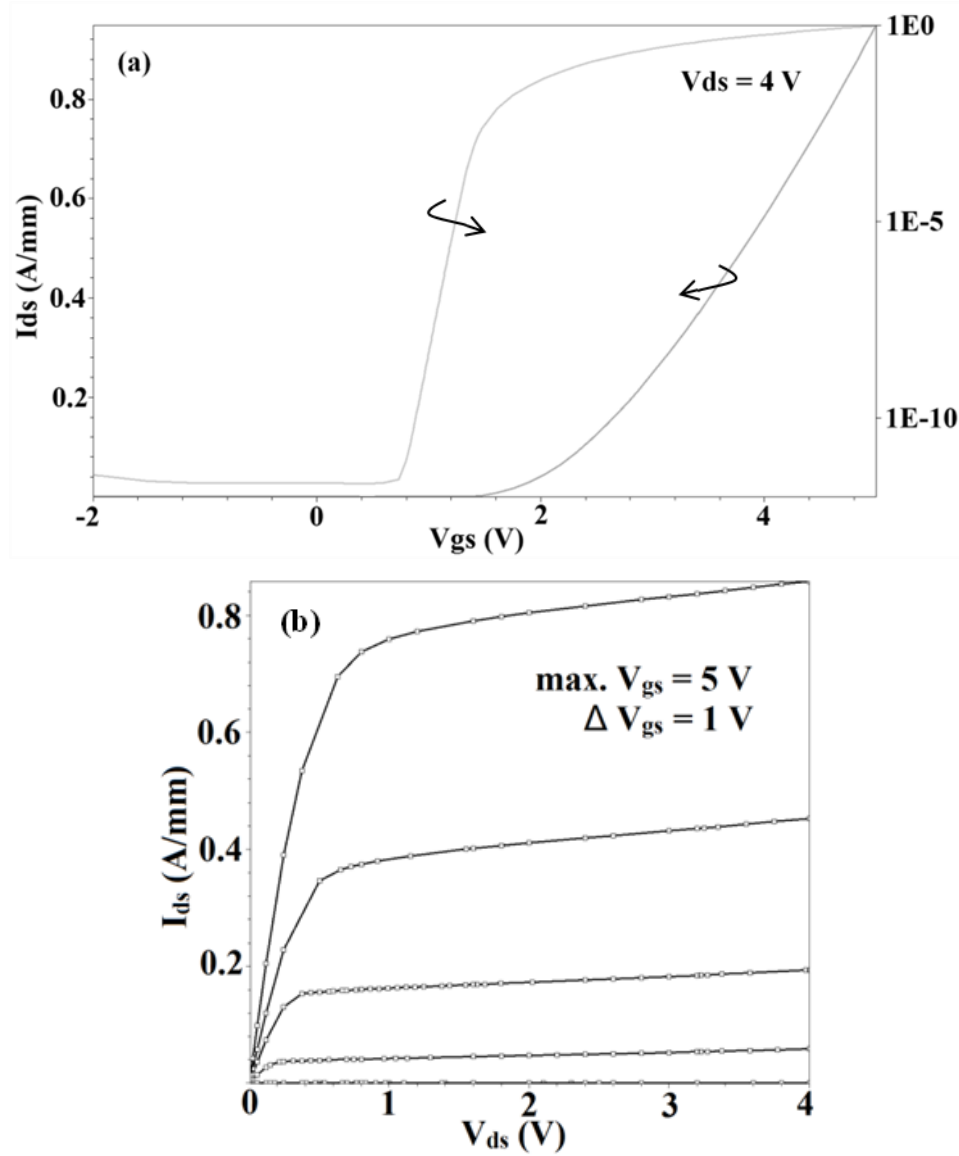


**Figure 5.5: Structure schematic of a single-channel MIS-HEMT**

The device simulation is first calibrated with experimentally measured electrical characteristics of E-mode N-polar GaN single-channel MIS-HEMT [97] to provide an insight into the nature of the channel development in the device. The AlN layers are set as undoped and thereby 2DEG results from the polarization charge distribution, which is simulated by spontaneous and piezoelectric polarization model. Fixed charges are inserted at the SiN/AlN interface to mimic passivation effect. Traps are introduced in the

GaN buffer layer for leakage current fine tuning. The gate workfunction is adjusted for threshold voltage calibration.

Figure 5.6 depicts the simulated device input and output characteristics, which are in good agreement with the experimental results [97].

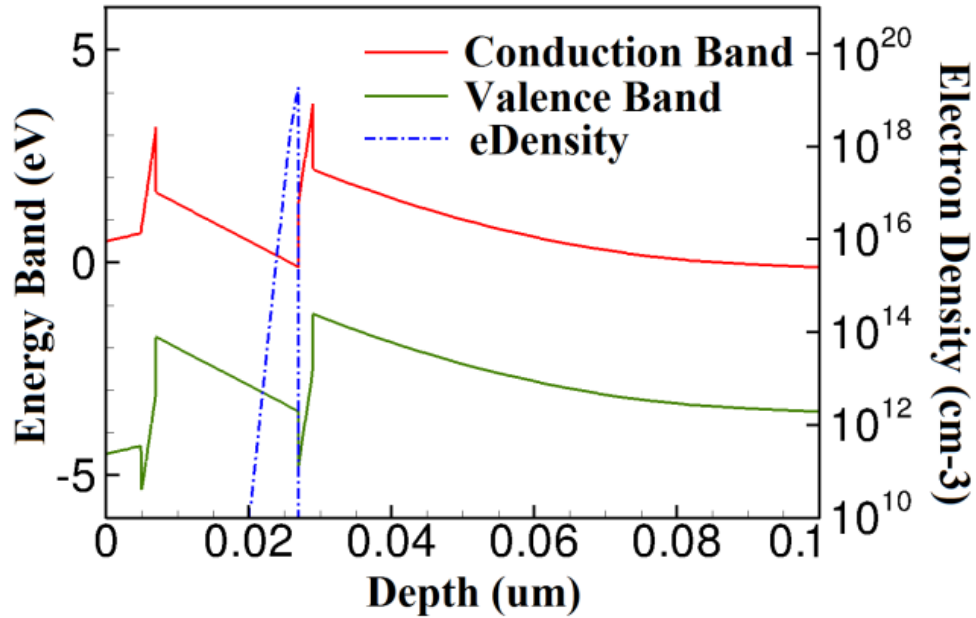


**Figure 5.6: Calibrated simulation results of (a) input and (b) output characteristics of a single-channel MIS-HEMT**

The simulated transfer  $I_d$ - $V_{gs}$  curve in Figure 5.6(a) shows the E-mode operation of the device with a threshold voltage  $V_{th}$  of 1.37 V under the bias condition  $V_{ds} = 4.0$  V.

Excellent subthreshold slope is obtained under the condition that gate leakage is not included in TCAD modeling. The simulated output  $I_d$ - $V_{ds}$  curves in Figure 5.6(b) show a maximum  $I_{ds}$  of 0.83 A at  $V_{gs} = 5.0$  V and  $V_{ds} = 4.0$  V. The slightly higher simulated output characteristics may be due to the smaller access region by ideal Ohmic contact assumption and heavily doped S/D region compared to the experimental structure.

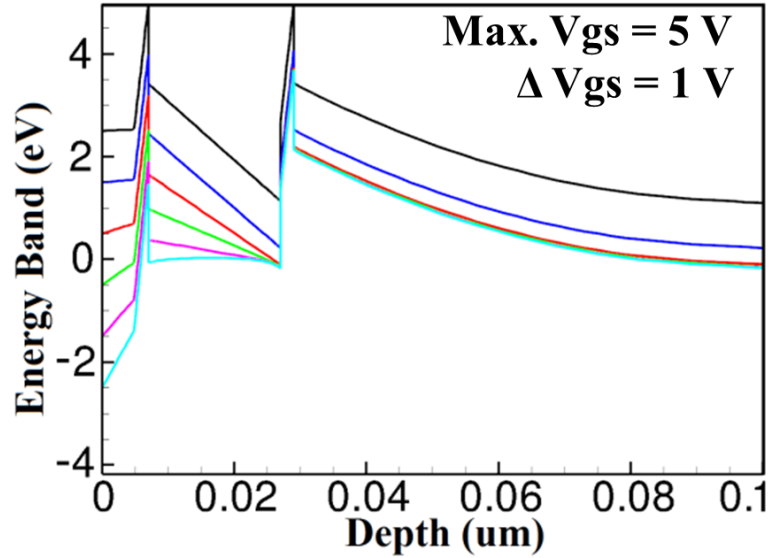
The simulated energy band diagrams and electron density distribution below the gate region are shown in Figure 5.7, whereas  $V_{gs}$  is set to be 2 V close to the threshold voltage and the 2DEG is induced at the order of  $10^{19}/\text{cm}^3$ .



**Figure 5.7: Energy band diagram and electron density for the single-channel HEMT under the bias where  $V_{gs} = 2.0$  V and  $V_{ds} = 0$  V**

Figure 5.8 includes the band diagrams of the E-mode single-channel MIS-HEMT versus the applied gate bias under zero drain bias. When gate bias is smaller than the threshold voltage, the 2DEG quantum well is away from the Fermi level, which indicates that the channel is not developed. As applied gate bias increases, the quantum well approaches and then dips into the Fermi level. This indicates the 2DEG channel is

gradually developed. As applied gate bias further increases, we noticed that the further movement of the quantum well will be limited since the 2DEG sheet density almost reaches its concentration limit. We also observe the conduction band close to the surface interface shifts downward toward the Fermi level as gate voltage increases. When  $V_{gs}$  reaches 5 V, the surface interface conduction band touches the Fermi level and provide a parasitic channel for the device conduction. This surface bending is consistent with the finding of Ref. [104] in which electron accumulation is observed at the gate dielectric and polarization semiconductor interface.



**Figure 5.8: Conduction band diagram under gate region versus gate bias for the single-channel HEMT**

#### **5.4 E-mode N-polar GaN Dual-Channel MIS-HEMT**

Suggested by the simulated band diagram discussed in single-channel device, we consider the possibility of the development of the surface inversion carrier channel in N-polar GaN layer. Due to the natural polarization direction property of N-polar GaN, the inversion carrier channel induced close to the surface interface, is separated from the



2DEG sheet confined close to the back one. This feature implies that the inversion carrier channel can be generated in addition to the 2DEG channel to form the dual conduction paths in one N-polar GaN layer.

With calibrated simulation models and reference single-channel device characteristics, E-mode N-polar GaN dual-channel MIS-HEMT is simulated and studied. To induce significant amount of electron density for inversion carrier channel in N-polar GaN layer, the gate controllability is needed to be strengthened. In this design, the single-channel device structure is further modified with a stack consisting of 10 Å SiN and 20 Å AlN virtually grown on the GaN. This gate dielectric scaling of MIS-HEMT device is similar to the idea of MOSFET gate oxide scaling, which is aimed at drain current enhancement and short channel effects improvement. Figure 5.9 describes the band diagram of the E-mode dual-channel HEMT versus gate bias. As applied gate bias increases, the bottom quantum well, due to the bandgap diagram discontinuities, approaches the Fermi level first. Then that quantum well is almost pinned at the Fermi level but the surface conduction band keeps shifting downward and start bending to form another “well” for additional conduction path. For thin gate dielectric stack, since the gate has a stronger impact on the surface, the “well” can dip into the  $E_F$  reference, which is consistent with the presence of higher electrons density close to the surface interface. This is also illustrated in Figure 5.10 where the device is under a 5 V gate bias and zero drain bias and each channel is individually induced with good confinement in one N-polar GaN layer, other than causing possible electron sheet overlap in Ga-polar GaN device, where the scattering will be worsen and thereby the carrier mobility will be reduced.

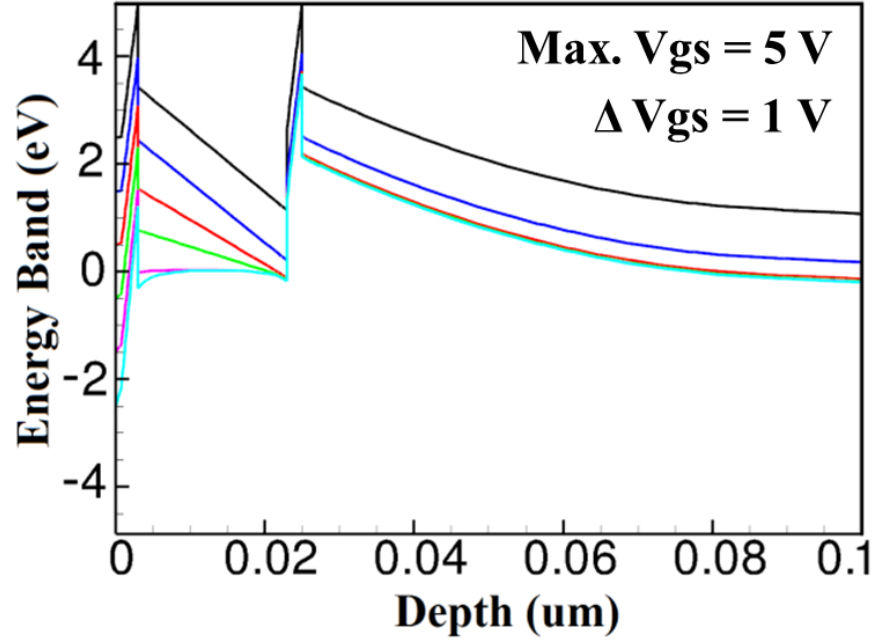


Figure 5.9: Conduction band diagram under gate region versus gate bias for the dual-channel HEMT. Inversion carriers accumulate at the GaN surface.

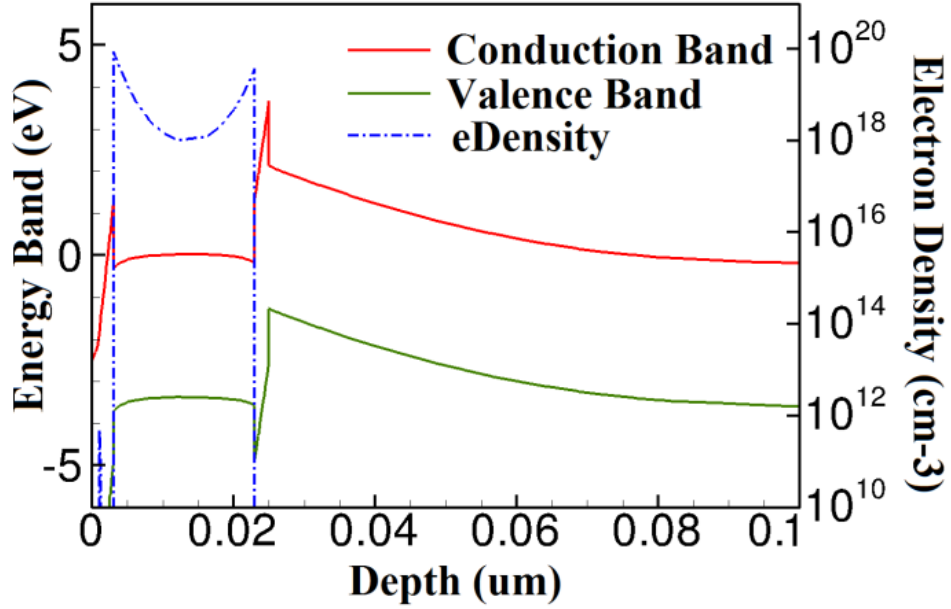
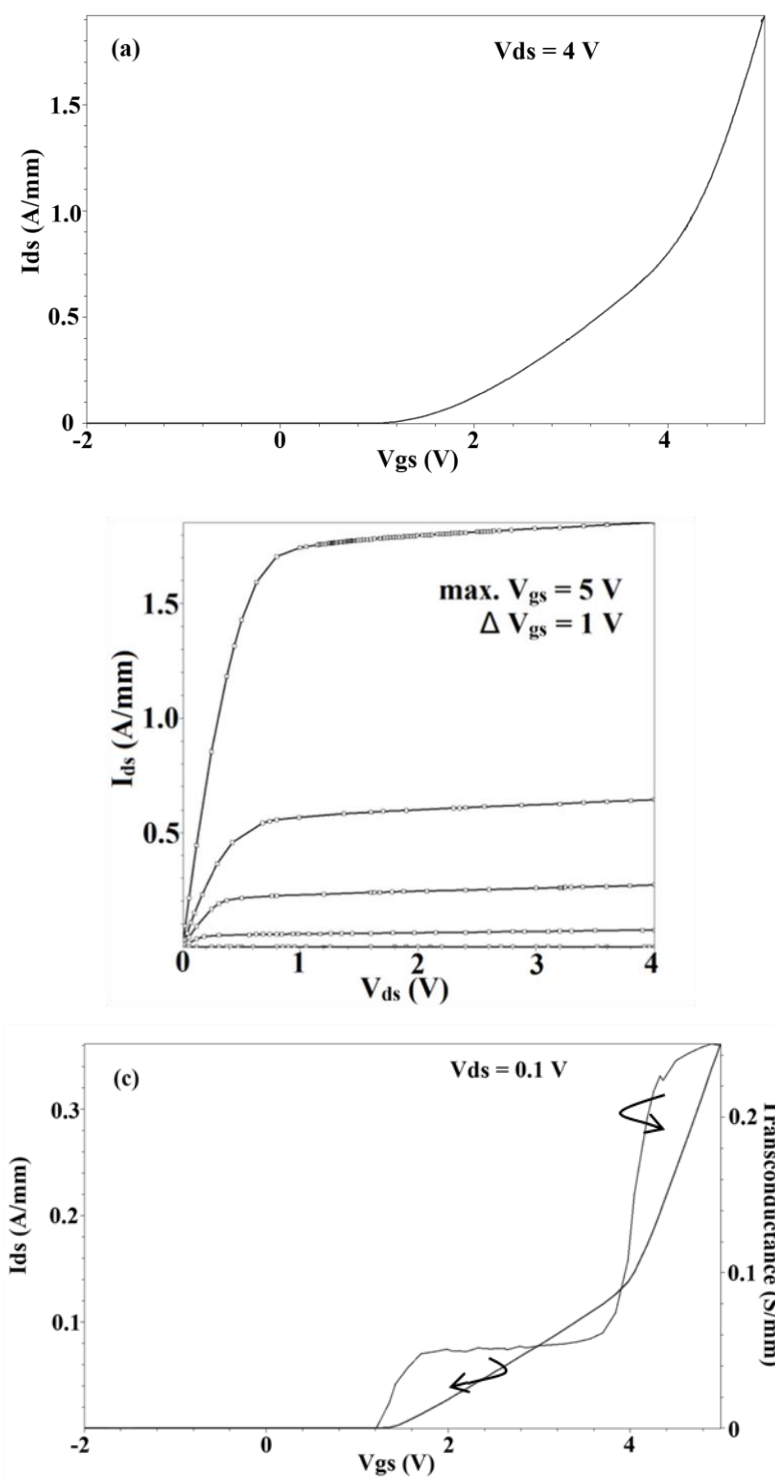


Figure 5.10: Energy band diagram and electron density for the dual-channel HEMT under the bias where  $V_{gs} = 5.0$  V and  $V_{ds} = 0$  V. Good confinement of each channel is observed.

The simulated input and output characteristics of the dual-channel MIS-HEMT are presented in Figure 5.11.



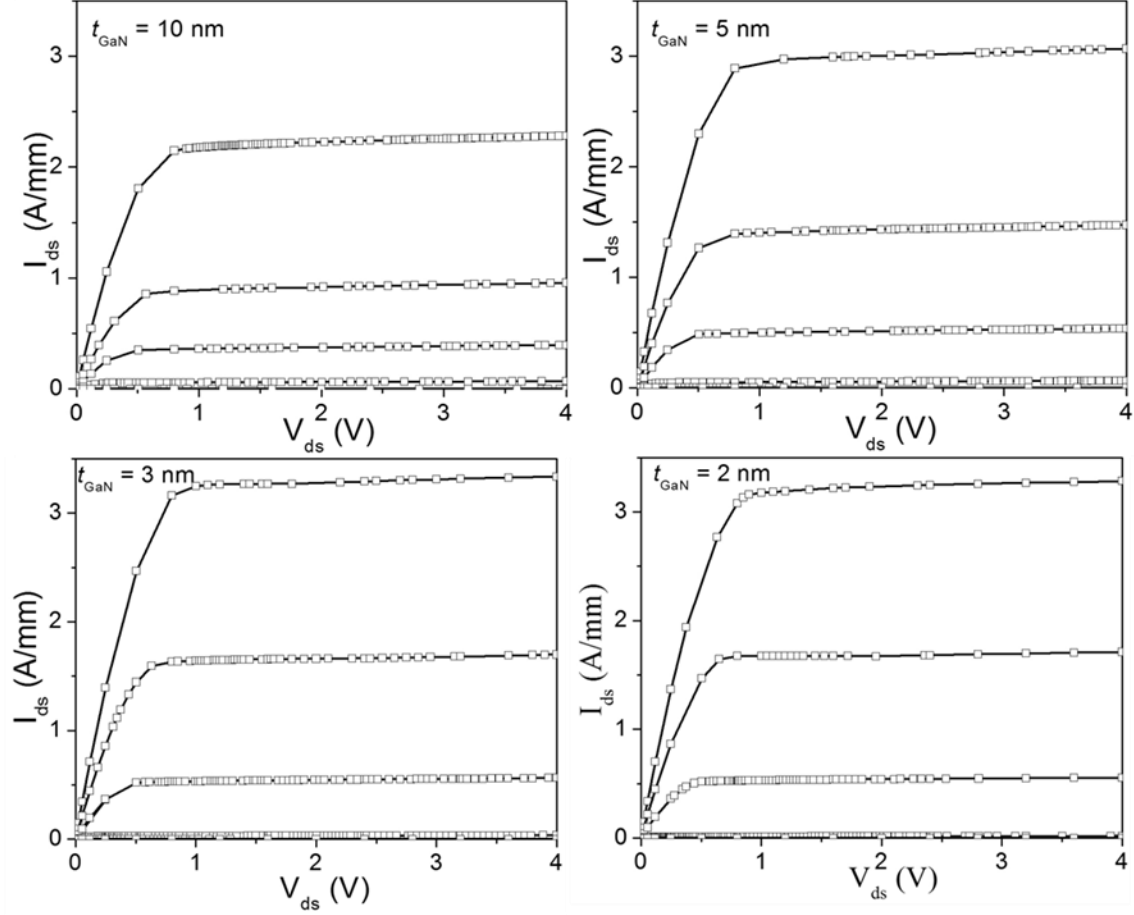
**Figure 5.11: Calibrated simulation results of (a) input, (b) output characteristics, (c) double peak gm curve of a dual-channel MIS-HEMT**

The input transfer curve shows a threshold voltage of 1.36 V as the single-channel device but a higher drive current compared to the single-channel input characteristic.

These are consistent with our aforementioned analysis. The 2DEG induced procedure has less to do with the gate dielectric and therefore its formation is similar to the one in single-channel device. Since the surface inversion channel is generated after the 2DEG, therefore the 2DEG development will determine the threshold voltage and thus the single-channel and dual-channel structure in this paper shares the same threshold voltage. When a positive enough gate bias is inserted, dual-channels will give a boost to the drive current. As illustrated in the output characteristic, dual-channel MIS-HEMT shows a normalized maximum drive current of 1.83A/mm, which is almost 2X maximum drive current as the single-channel device. The inversion carrier channel significantly enhances the device current carrying capability.

It is noted that the transconductance curve in Figure 5.11(c) shows two peaks as the gate voltage ramps up to 5 V. This also illustrates the dual channel development procedure. The 2DEG channel is formed ahead of the inversion carrier channel as the quantum well touches the Fermi level earlier than the surface conduction band bends downward to the Fermi level.

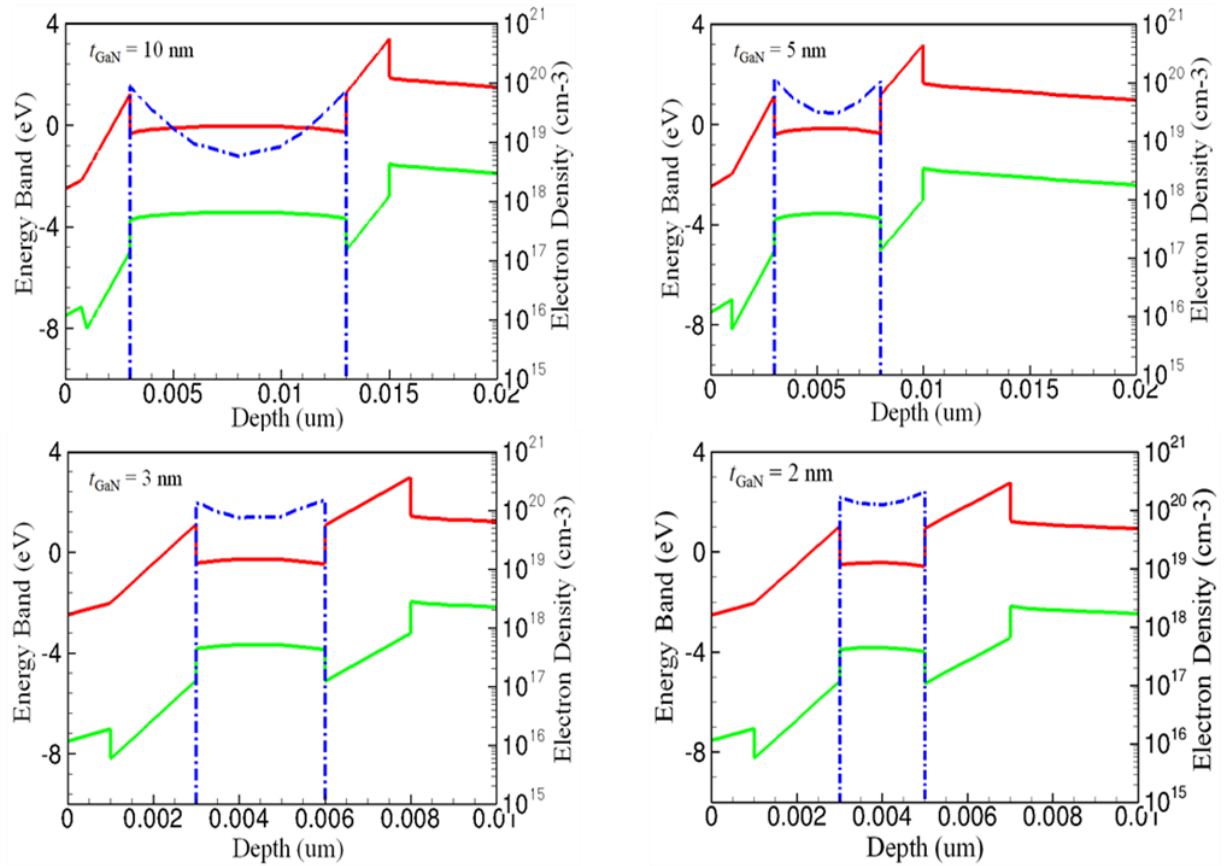
Correspondingly,  $g_m$  reaches its first peak when 2DEG density achieves its maximum value and then it approaches its second peak as the inversion carriers start to accumulate close to surface interface. The dual-peak feature of the dual-channel HEMT is believed to be due to the asymmetrical channel formation. Threshold voltage tuning may synchronize the channel development and leads to the merging of the two peaks to form a continuous monotonous  $g_m$  curve. However, the linearity of  $g_m$  still needs to be improved. Optimization of transconductance linearity is under investigation.



**Figure 5.12: Output Characteristics of the 0.62  $\mu\text{m}$  gate length with various  $t_{\text{GaN}}$ . Device features maintain good confinement for each channel ( $V_{\text{gs}} = 5 \text{ V}$   $\Delta V_{\text{gs}} = 1 \text{ V}$ ). Degradation is observed in the device with  $t_{\text{GaN}} = 2 \text{ nm}$ .**

To further improve the drive current, vertical scaling and optimization of GaN layer thickness is performed by conducting study with another four different GaN layer thicknesses ( $t_{\text{GaN}} = 10 \text{ nm}$ , 5 nm, 3 nm, 2nm) and the corresponding impact on the device characteristics is studied. As the GaN layer thickness shrinks, the surface inversion carrier density is not much affected but the bottom 2DEG density increases due to reduction in its distance to the gate electrode. Improved output characteristics are observed as in Figure 5.12. Results also illustrate that as the  $t_{\text{GaN}}$  thickness scales down to 3 nm,  $I_{\text{max}}$  reaches 3.34 A/mm. This enhancement also benefits from the double heterojunction structure, the N-polar GaN layer and the layer scaling since these help to

minimize the 2DEG channel overlap and reduce the carrier-to-carrier scattering. However, as  $t_{\text{GaN}}$  is reduced to 2 nm, the output characteristics start to degrade and the threshold voltage ramps up. The significant channel overlap, as shown in Figure 5.13, results in the decrease of the mobility and therefore put a restriction on the drive current. For experimental device, more degradation on the carrier mobility is expected due to the interface scattering and surface roughness, which is not included in this TCAD simulation due to the unavailability of related GaN models.



**Figure 5.13: Energy band diagram and electron density for the dual-channel HEMTs with various  $t_{\text{GaN}}$  under the bias where  $V_{\text{gs}} = 5.0$  V and  $V_{\text{ds}} = 0$  V. Significant channel overlap is observed.**

## 5.5 Summary

We have demonstrated a design method of E-mode N-polar GaN single-channel and dual-channel MIS-HEMTs. The mechanism for the creation of the additional inversion carrier channel has been identified. The accumulated electrons close to the interfaces and double peaks of the  $g_m$  demonstrate the existence of the dual channels. We have shown that the N-polar GaN is suitable for dual-channel MIS-HEMT because the location of the natural 2DEG induced at the back barrier interface helps reduce the dual-channel overlap. Significant increase in the on-state current and thereby increased output power density and RF amplification capability suggests that the E-mode N-polar GaN dual-channel MIS-HEMT can be a promising device structure for RF/power amplifier application. In addition, we have demonstrated the design and optimization method of E-mode N-polar GaN dual-channel MIS-HEMT. Scaling of the GaN layer increases the bottom 2DEG density while maintaining good confinement for both channels. However, aggressive scaling will introduce channel overlap and possible interface scattering, which would degrade device characteristics.

# Chapter 6

## TCAD Prediction of InGaAs MOSFET

### 6.1 Promising InGaAs material

Besides the wide bandgap III-V material GaN with high breakdown electric field and high saturated electron velocity, another type III-V compound with narrow bandgap shows superior electron mobility because of its small effective mass. Table 6.1 compares the intrinsic properties of III-V compounds and silicon. InGaAs owns a comparable effective density of states in the conduction band as well as a superior electron mobility, making it a promising material for low-power high-performance applications judging by the current drivability according to the current density equation,

$$J_{on} = qn\mu E.$$

The favorable metrics of InGaAs are recognized by researchers that it is an alternative channel material for ultra-low power logic applications. In 2007, the Purdue University research team demonstrated an E-mode InGaAs nMOSFET with 0.5  $\mu\text{m}$  gate length and  $\text{Al}_2\text{O}_3$  gate dielectric. The threshold voltage was around 0.5 V and the drive current is at about 325  $\mu\text{A}/\mu\text{m}$  ( $V_d = 2$  V,  $V_g = 4$  V) [105]. Although this III-V high mobility device surpassed the silicon counterpart in the aspect of current drivability, the poor interface states and the large source/drain resistance prevented the narrow bandgap device from performance maximization.



**Table 6.1: III-V compound and silicon material properties at room temperature**

Parameters	InAs	In <sub>0.53</sub> Ga <sub>0.47</sub> As	GaAs	GaN	Si
$\epsilon_r$	15.1	13.9	13.1	8.9	11.9
$N_C$ (cm <sup>-3</sup> )	$8.7 \times 10^{16}$	$2.8 \times 10^{17}$	$4.7 \times 10^{17}$	$2.3 \times 10^{18}$	$2.8 \times 10^{19}$
$N_V$ (cm <sup>-3</sup> )	$6.6 \times 10^{18}$	$6.0 \times 10^{18}$	$7.0 \times 10^{18}$	$4.6 \times 10^{19}$	$1.0 \times 10^{19}$
$E_G$ (eV)	0.35	0.7	1.424	3.4	1.12
$m_e^*/m_0$	0.023	0.041	0.067	0.2	0.26
$\mu_n$ (cm <sup>2</sup> /V-s)	25000	7000	4000	1000	800
$\mu_p$ (cm <sup>2</sup> /V-s)	500	300	250	30	400
$v_{sat}$ (m/s)	$4 \times 10^7$	$7 \times 10^6$	$8 \times 10^6$	$2.5 \times 10^7$	$8 \times 10^6$

To fully utilize advantages of InGaAs, researchers proposed different techniques to optimized device characteristics. Recent focus lies in the mobility enhancement and the leakage suppression. The former can be realized by reducing carrier effective mass, improving interface condition or introducing lateral tensile strain in the channel. In 2008, the Purdue University research team improved InGaAs MOSFET device performance by incorporation of a high quality gate oxide and a richer indium content InGaAs channel layer [106]. This 0.4  $\mu\text{m}$  gate length device showed a threshold voltage of 0.4 V, a drive current over 1 A/mm ( $V_d = 2$  V,  $V_g = 4$  V), and suppressed gate leakage current. Yeo's Goup in National University of Singapore proposed a different approach in 2009. They adopted a selective epitaxy of in-situ doped In<sub>0.4</sub>Ga<sub>0.6</sub>As source/drain region which has a lattice mismatch to the In<sub>0.53</sub>Ga<sub>0.47</sub>As channel region. The heavy doped S/D region enabled small Ohmic contact while the induced lateral strain improved the carrier mobility [107].

Extensive research works have been carried out for leakage current suppression. In 2009, research team from Purdue University demonstrated the first well-behaved inversion-mode InGaAs FinFET with improved short channel effect managements. The

enhanced electrostatic gate control over the channel improved subthreshold swing and reduced DIBL [108]. Later on, Yokoyama's group showed aggressively suppressed leakage current by employing the InGaAs-on-insulator structure with an ultra-thin-body and a double-gate control. The record high  $I_{\text{on}}/I_{\text{off}}$  ratio was about  $10^7$  [109].

In addition to the efforts made to InGaAs MOSFET, InGaAs HFET was also explored and developed. In 2011, Intel showed their latest InGaAs HFET with multi-gate structure [24, 25]. The gate length was scaled down to 60 nm while the fin thickness was reduced to 30 nm. Benefitting from the multi-gate structure, the SCEs are successfully suppressed. Reported SS and DIBL are 95 mV/dec and 50 mV/V respectively, which are less than half of the planar InGaAs FET in the same dimension scale.

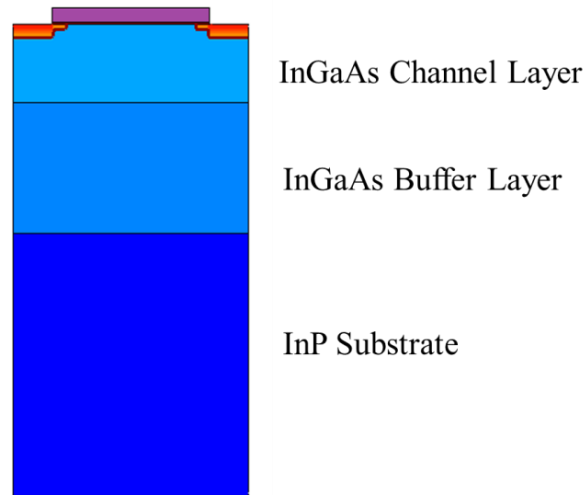
It is understood that the cost of the fabrication of InGaAs device is extremely expensive and the scaling of this novel transistor will be very challenging due to immature process techniques and insufficient understandings of device physics. To explore the device potential for low-power high-performance applications and to gain the physics insight of InGaAs transistors, we propose to build the device in the TCAD foundry to fully examine the device characteristics and to set the upper limit for the device performance.

In this chapter, the focus is on InGaAs MOSFET which is compatible to the CMOS fabrication process. The transistor will be first constructed with a 2-D planar structure. The calibration will be performed through the design of experiments benchmarking published data by Ye's team [105]. Important device parameters which have significant impact on device characteristics are identified in this work. The scaling potential of the planar InGaAs MOSFET to 22 nm technology node, where the mass production has not

reached yet, is investigated for understanding the challenges and opportunities of such a device. The nanometer scale InGaAs FinFET is also explored and modeled by 3-D TCAD simulation. And the corresponding results are discussed.

## 6.2 TCAD Simulation of Planar InGaAs nMOSFET

The planar InGaAs nMOSFET structure studied in this chapter is shown in Figure 6.1 which has the similar experimental structure described in reference [105]. The channel layer consists of a 300-nm-thick  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  material with a p-type doping at  $10^{17} \text{ cm}^{-3}$ , on top of a p-type doped ( $4 \times 10^{17} \text{ cm}^{-3}$ ) 500-nm-thick  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  buffer and a 1- $\mu\text{m}$ -thick heavily doped p-type InP substrate. The gate length is set to be 0.5  $\mu\text{m}$  first to benchmark the experimental results.



**Figure 6.1: Simulated cross-sectional schematic of the planar InGaAs MOSFET**

Considering the feasibility of Ohmic contact [107, 110] and the robustness of simulation, the simulations assume perfect contact condition on S/D region. However, a parasitic resistance for tuning purpose is attached to S/D regions to account for the contact resistance and the mobility degradation in the channel. To present a comprehensive device TCAD modeling, we include the interface states which are known

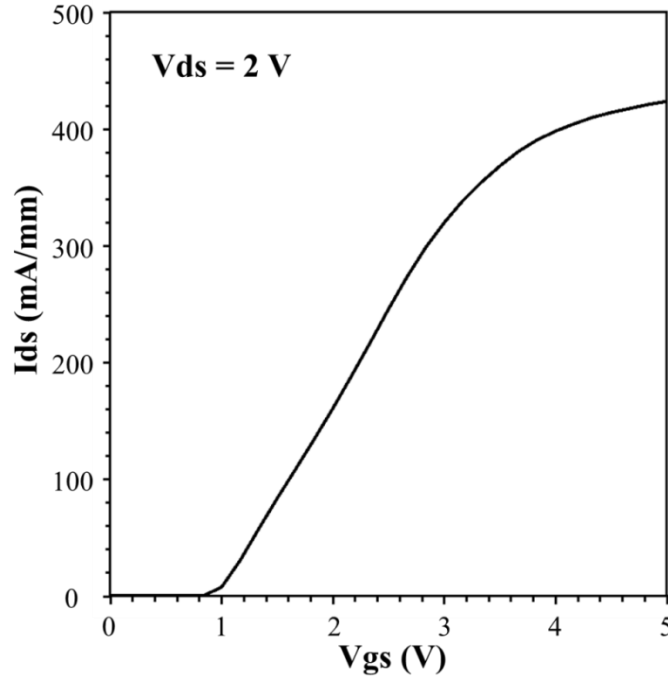
as high density defects, comparable to the effective density of states in conduction band and capable of greatly stalling the electron transportation. However, due to the controversial physical understandings of traps, the lack of related measurement data and the simulation convergence issue, only a single level donor-like trap and an acceptor-like one are inserted. The magnitude of the density and the energy level follow the measurement data. Nevertheless, by making those reasonable assumptions, the TCAD modeling should provide a fair visualization of the promising InGaAs device.

A number of physics models are included to address the concerns on mobility degradation. Besides the trap models, the Fermi statistical function suitable for high carrier density, the Arora Model describing the doping-dependent mobility in III-V compound, the hydrodynamic transport model accounting for the rigorous carrier conduction and self-heating issue at high current density, and the high field saturation model are implemented towards the simulation of InGaAs devices. In addition, as the shrinking of the device dimension approaches to quantum mechanical length scales, the density gradient quantization model will be adopted to reflect the carrier quantization nature.

Device electrical behavior and physical properties such as electrostatic potential, input and output characteristics, and band diagrams are examined. After the successful completion of the virtual device fabrication of the reference device, optimization will be performed with the consideration of short channel effects and drive current as the device is scaled down to 100 nm and 22 nm node.

The simulation of 0.5  $\mu\text{m}$  gate length reference structure is calibrated by tuning the mobility model, trap model and two other fitting parameters, the gate workfunction and

the source/drain series resistance  $R_{SD}$ . The carrier mobility model and the inserted traps need to adapt the experimental measurement data. The gate workfunction is adjusted for threshold voltage calibration. The series resistance, which accounts for the parasitic resistance such as contact resistance, extrinsic component, alters the on-state current.

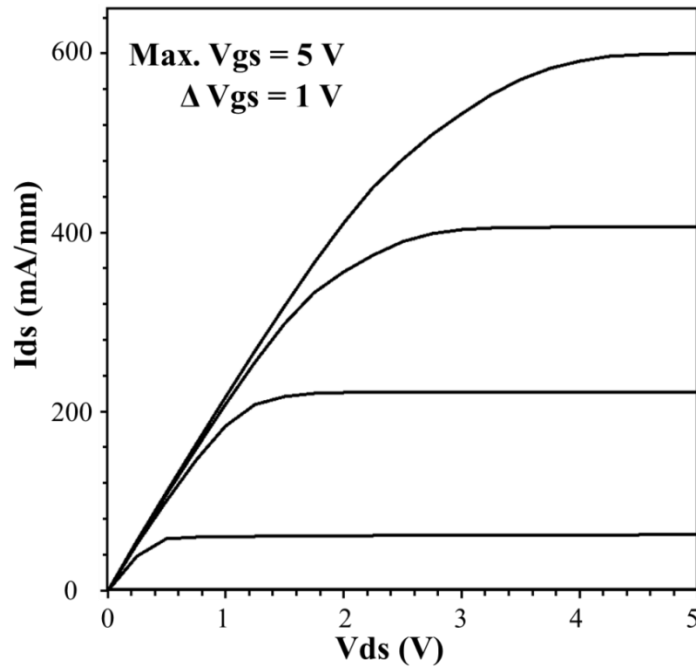


**Figure 6.2: Calibrated simulation results of input characteristics of a 0.5  $\mu\text{m}$  gate length InGaAs n-type MOSFET**

The calibrated input characteristics in Figure 6.2 agree with the experimental results in reference [105]. For the simulated device at a drain bias of 2 V, the threshold voltage is 0.83 V and the transconductance is observed at 172 mS/mm. However, the extracted subthreshold swing and DIBL, 125 mV/dec and 75 mV/V respectively, are half of the reference results. The differences are due to the preliminary trap model which only includes a single level acceptor trap at the density of  $6.5 \times 10^{12} \text{ cm}^{-2}$  and a single level donor trap at  $5 \times 10^{13} \text{ cm}^{-2}$ . This simplified method resulted from the measurement limitation and data availability. Despite the state-of-the-art trap model for III-V material

is not well developed, we still include the trap model in the TCAD modeling to provide reasonable upper projection of InGaAs transistor.

We also noticed that SCEs for InGaAs MOSFET are worse than the silicon counterpart. This is understandable due to the fact that the unoptimized source/drain extension region along with small junction barrier height of InGaAs widens the depletion region at source/bulk junction. The drain bias weakens the gate control in inducing electron in the channel. The  $I_{ds}$ - $V_{ds}$  group curves shown in Figure 6.3 have a fair quantitative agreement with the experimental results. A high  $I_{max}$  of 600 mA/ $\mu$ m is demonstrated.

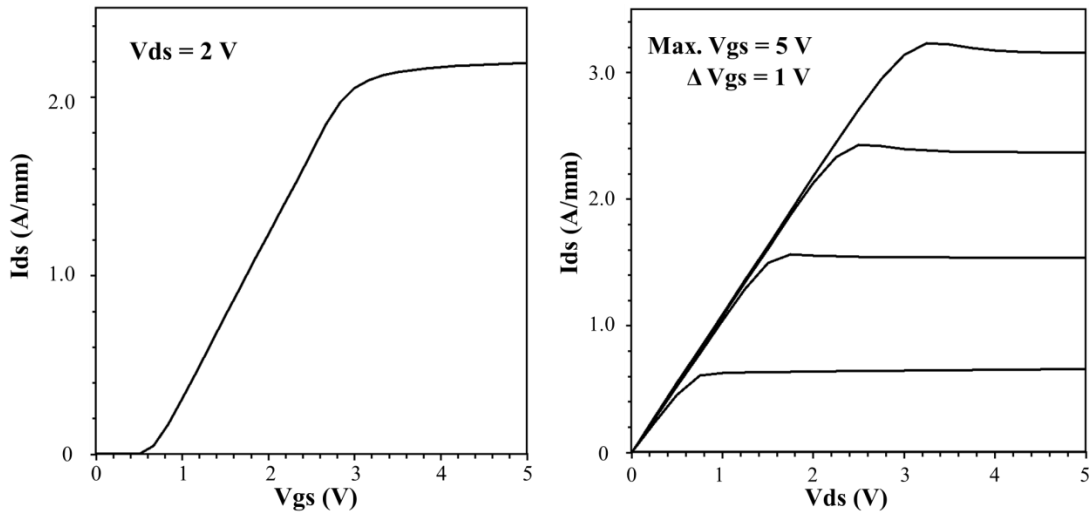


**Figure 6.3: Calibrated simulation results of output characteristics of a 0.5  $\mu$ m gate length InGaAs n-type MOSFET**

Following the general constant field scaling guideline, the primary device scaling variables for the modeled InGaAs devices are gate length  $L_{gate}$ , bulk doping concentration  $N_{bulk}$ , gate dielectric layer thickness  $t_{ox}$ . If the scaling factor for  $L_{gate}$  is  $1/K$ , then the ratio for doping concentration will be  $K$ . It is noted that for  $t_{ox}$  we intend not to follow the

scaling ratio but specify a fixed thickness for different technology node because in real device the gate dielectric should keep at a certain thickness to suppress the gate leakage.

Accordingly, for a 100 nm node InGaAs nMOSFET, we set the gate length at 100 nm, fin width at 40 nm, Al<sub>2</sub>O<sub>3</sub> gate dielectric thickness at 5 nm, and the bulk doping at  $5 \times 10^{17} \text{ cm}^{-3}$ . The source/drain extension region length  $L_{\text{ext}}$  is also reduced to 30 nm. For a 22 nm node one, we set  $L_{\text{gate}} = 25 \text{ nm}$ ,  $W_{\text{fin}} = 10 \text{ nm}$ ,  $N_{\text{bulk}} = 2 \times 10^{18} \text{ cm}^{-3}$ ,  $t_{\text{ox}} = 5 \text{ nm}$  and  $L_{\text{ext}} = 10 \text{ nm}$ . The simulated input and output characteristics for these two devices with different dimensions are shown in Figure 6.4 and Figure 6.5, respectively.

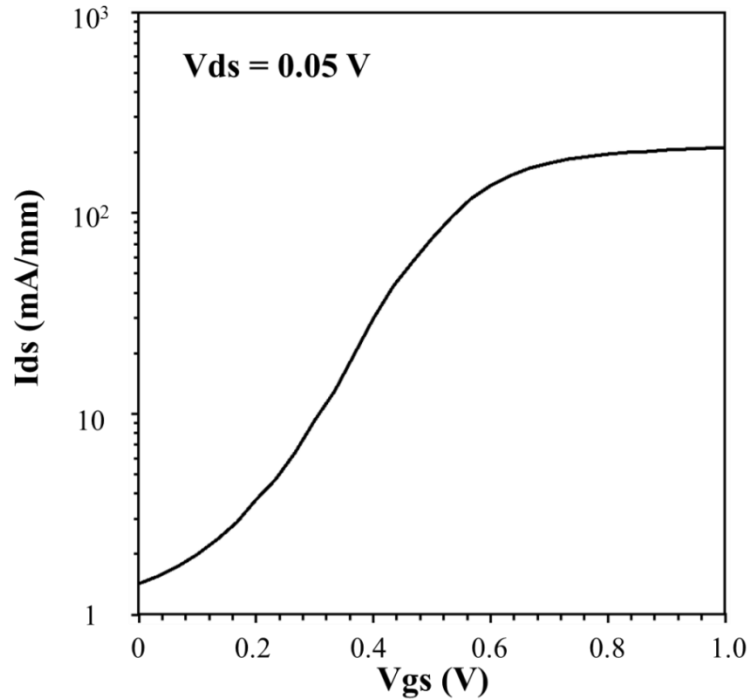


**Figure 6.4: Calibrated simulation results of input and output characteristics of a 100 nm gate length InGaAs n-type MOSFET.**

The 100 nm gate length InGaAs MOSFET shows a small threshold voltage of 0.6 V and the maximum normalized drive current is more than four times of the 0.5  $\mu\text{m}$ . And these results satisfy the scaling prediction. The extracted SS and DIBL are 150 mV/dec and 90 mV/V.

Although we are not surprised to see the degraded SS and DIBL, those short channel effects actually will become the barriers to the integration of InGaAs MOSFET for logic

application as aggressive scaling continues. This is demonstrated by the TCAD modeling results of the 22 nm node InGaAs MOSFET.



**Figure 6.5: Calibrated simulation results of input characteristics of a 25 nm gate length InGaAs n-type MOSFET**

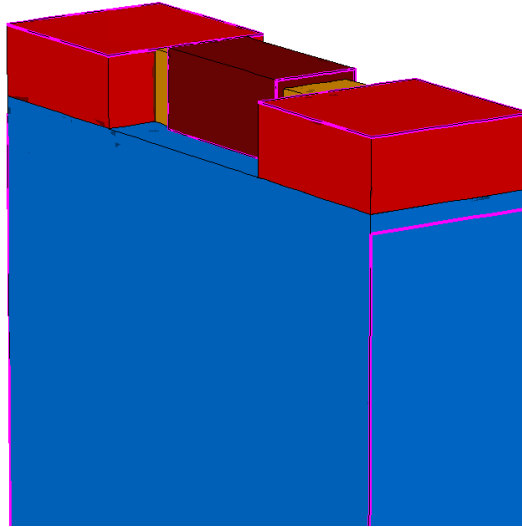
The tiny device is biased under a lower voltage operation since a high voltage will cause severe leakages for a high mobility transistor. In addition, the gate workfunction is changed from 4.2 eV to 4.6 eV for this case to alleviate the drain competition against the gate in channel control. Even with those efforts, SCEs distort the transistor function. Under 0.05 V drain bias, the normalized leakage current is in the magnitude of 1 mA/mm and the extracted SS is more than 300 mV/dec. This is due to the intrinsic small junction barrier height of InGaAs MOSFET. A structure with enhanced gate control is desirable to suppress SCEs for this tiny device. The output characteristics which is not shown here is more like an illustration of a resistor especially when the drain bias become large. New structure is desired to correct the device performance.



### 6.3 3-D TCAD modeling of InGaAs FinFET

Inspired by the silicon FinFET technology, to aggressively suppress SCEs for nanoscale InGaAs device, we have applied 3-D multi-gate structure to enhance the gate control over the channel.

The non-planar InGaAs nMOSFET structure studied in this chapter is shown in Figure 6.6 which takes the similar experimental structure described in reference [108]. The p-type lightly doped ( $2 \times 10^{16} \text{ cm}^{-3}$ ) fin is set with a dimension where fin width and height are both 40 nm. A 5 nm  $\text{Al}_2\text{O}_3$  is conformally deposited on the fin and it is wrapped by a 100 nm long gate contact. The fin, virtually epitaxially grown on heavily doped InP buffer and substrate, connects the raised source and drain region.



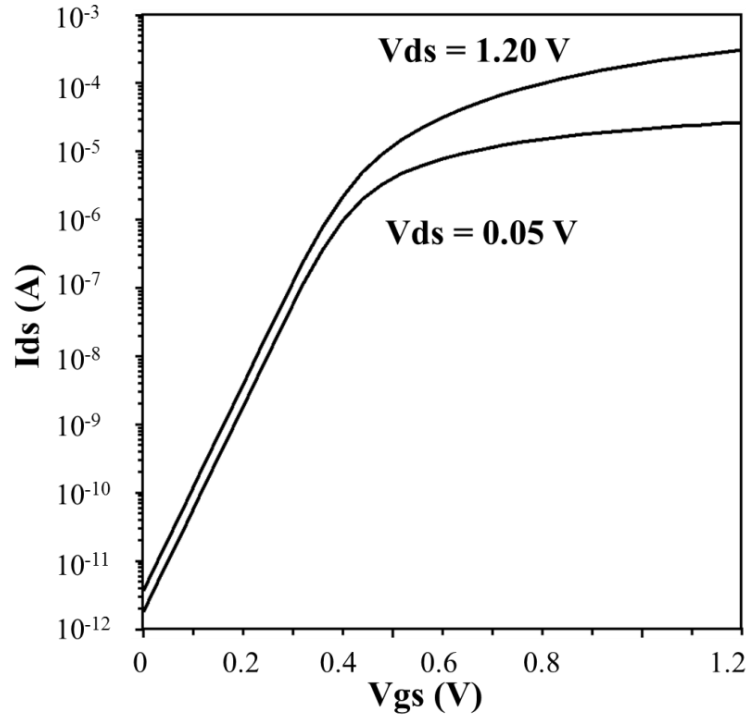
**Figure 6.6: 3-D InGaAs FinFET structure for TCAD modeling**

The computational effort for this 3-D structure is much larger than the 2-D cross sectional one because the non-planar structure involves more than 20 times of mesh elements of the planar structure. It also should be noted that the InGaAs material property parameters and transport model are not well developed at this moment. Therefore, the 3-

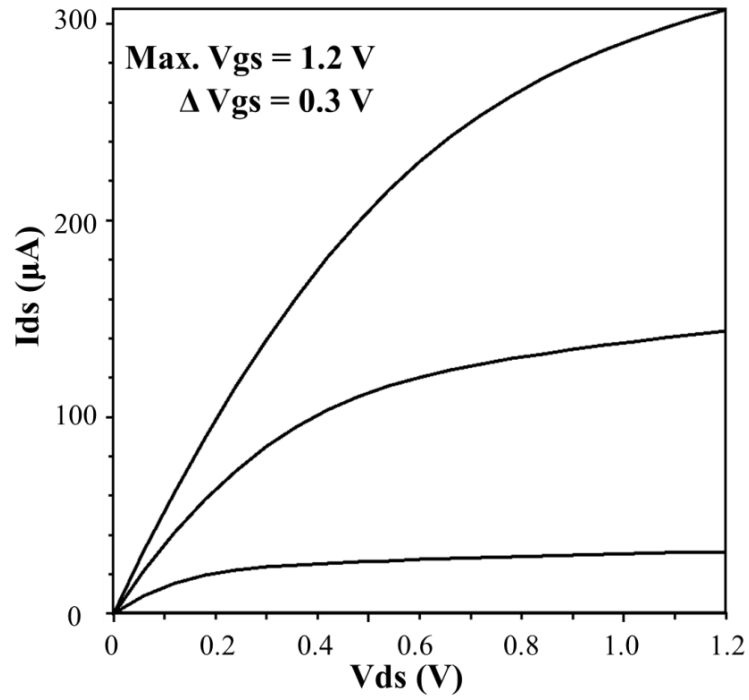
D simulation results based on model approximation and numerical solution only serve as trend predictions for the InGaAs n-type FinFET device.

To provide upper limit projections of InGaAs FinFET through TCAD modeling, we assume perfect Ohmic contact and turn interface states impacts into mobility degradation. This assumption is also due to the poor available trap data due to the limited measurement techniques. A constant mobility model is adopted at the high peak value of  $2200 \text{ cm}^2/\text{V s}$  in the simulation. For the continuity equation, we activate both the hydrodynamic transport model and carrier quantization model for this high performance nanoscale device. After the examination of the 100 nm gate length InGaAs FinFET, the device will be scaled down to 22 nm node as well to explore its potential.

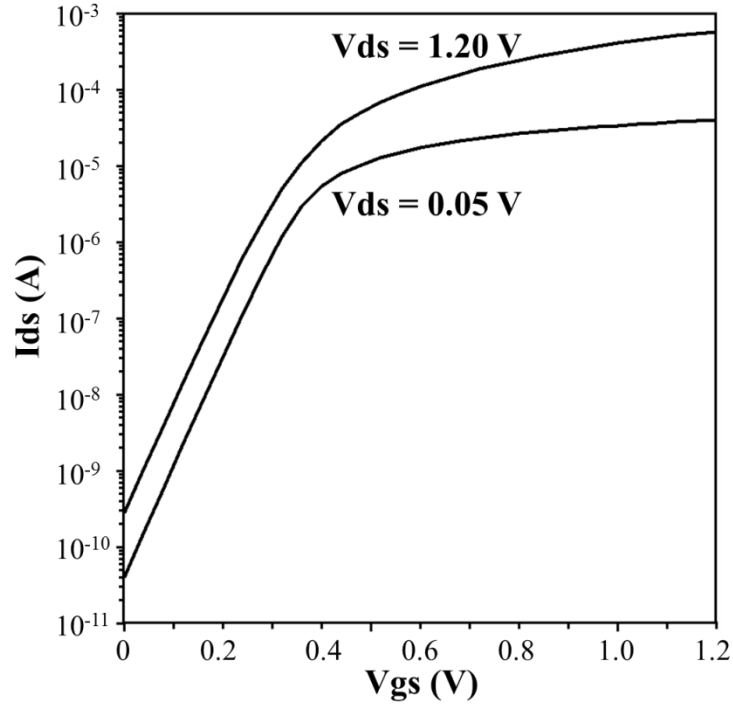
The simulation of the 0.1  $\mu\text{m}$  gate length reference structure is also calibrated by tuning two fitting parameters, the gate workfunction and the source/drain series resistance  $R_{\text{SD}}$ . The input and output characteristics (see Figure 6.7 and Figure 6.8) fairly agree with the experimental results in reference [108]. The simulated threshold voltage is 0.37 V at a drain bias of 1.2 V and the on-state current  $I_{\text{max}}$  is 300  $\mu\text{A}$  for a 120 nm 3-D channel width. The normalized maximum current is over 2.4 A/mm, which is approximately 10 times that of the FinFET performance discussed in Chapter 3. In addition, thanks to the multi-gate structure, the SCEs are suppressed. Extracted results show improved SS and DIBL which are 67 mV/dec and 40 mV/V respectively.



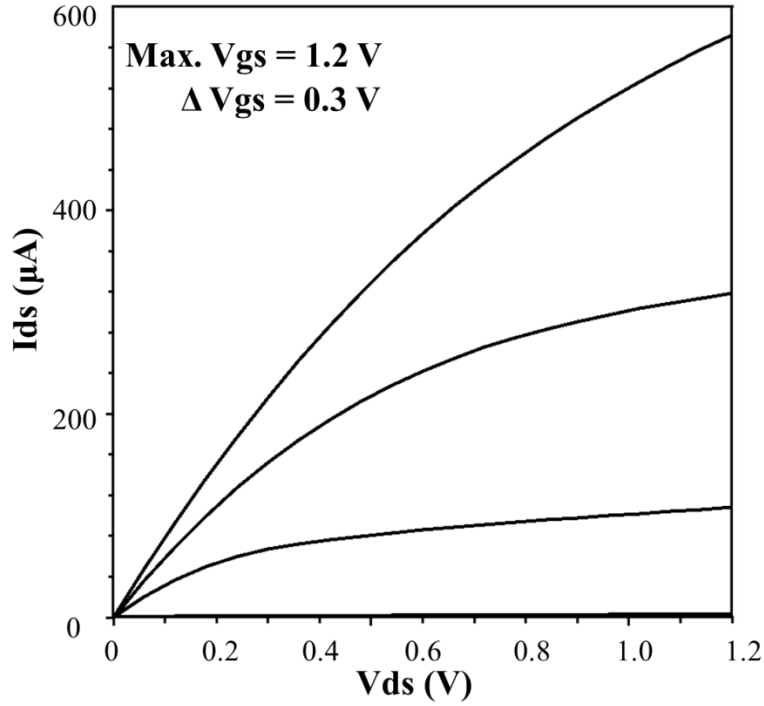
**Figure 6.7: Calibrated 3-D simulation results of input characteristics of a 100 nm gate length InGaAs n-type FinFET**



**Figure 6.8: Calibrated 3-D simulation results of output characteristics of a 100 nm gate length InGaAs n-type FinFET**



**Figure 6.9:** Calibrated 3-D simulation results of input characteristics of a 25 nm gate length InGaAs n-type FinFET



**Figure 6.10:** Calibrated 3-D simulation results of output characteristics of a 25 nm gate length InGaAs n-type FinFET

Improved SCEs are also observed in a 22 nm node InGaAs FinFET, which has a 25 nm gate length and 10 nm fin width. The simulation results in Figure 6.9 and Figure 6.10 show a steep subthreshold slope with  $SS = 69$  mV/dec and a good  $I_d$ - $V_d$  group curves. At a drain bias of 1.2 V, the threshold voltage is 0.31 V. The DIBL is found to be 56 mV/V, much lower than the one obtained from planar structure. The extracted normalized  $I_{\max}$  from the output characteristics in Figure 6.10 is 6.36 A/ $\mu\text{m}$  (an on-state current of 572  $\mu\text{A}$  based on a 3-D channel at 90 nm), which indicates a great potential for InGaAs FinFET towards low-power high-performance application.

TCAD simulations show that the FinFET structure using InGaAs material can achieve high drive current and improved SCEs with interface states minimized.

## 6.4 Summary

The TCAD modeling of planar and non-planar InGaAs MOSFET supports that this narrow bandgap III-V transistor is a promising device beyond silicon technology. The superior carrier transport properties leads InGaAs to pursue more than 10 times of the drive current than the silicon counterpart even under low voltage bias.

Short channel effects are the critical issues that need careful attention for InGaAs MOSFET. Similar to silicon technology, as the shrinking continues, structure and doping optimization along with new process techniques are required for InGaAs transistor to become commercially sustainable in the nanometer scale. In this chapter, TCAD simulation results demonstrate 3-D fin structure can greatly improve SCEs while maintaining an excellent current drivability.

# Chapter 7

## Conclusions

### 7.1 Summary

Moore's Law witnesses the development of the silicon technologies in the past four decades. As the device shrinking enters into nanoscale regime, short channel effects, process random variation and fabrication complexity stall the transistor density increase rate. To overcome those challenges in the post-Moore era, new trends of solid state electronics advancement are proposed by ITRS: the continuous scaling of digital functionalities, the progress of diversified non-digital functionalities and the heterogeneous integration of both functionalities into a compact system. These new directions of development urge the research efforts on non-classical transistors. The novel 3-D silicon FET maintains the miniaturization of physical feature sizes for CMOS technology. New gate stack materials which have high electron saturated velocity and high breakdown electrical field are favored for RF/power applications where traditional silicon technologies meet the bottlenecks. And high mobility channel materials are promising candidates for the planar device aiming at the low-power high-performance application.

To gain the visualization of emerging device technologies, TCAD is a powerful and efficient tool in the development of the semiconductor process and the simulation of device electrical behaviors. In this dissertation, Synopsys Sentaurus TCAD is used to design non-classical field effect transistors, to get clearer picture of the device physical

insights and validate device physics understandings, and explore the interaction between devices and circuits under various applications.

The TCAD modeling methodology utilized in this research work enriches multiple ways the fundamental knowledge base necessary to design both novel silicon and III-V compound devices that are capable of satisfying the multi-functional needs demanded by the dual trends “More Moore” and “More than Moore” in the new era.

For the silicon technology, the quasi-planar 3-D transistor FinFET, with the innovative device structure, demonstrates enhanced gate controllability and thereby suppressed SCEs than the planar MOSFET. Furthermore, compatibility with the CMOS process technology makes it as a promising alternative device in sub-32 nm regime.

This dissertation provides application-oriented design considerations and optimization guidelines for silicon FinFET through extensive device simulations. For digital applications with the concern of heating impact, 3-D TCAD modeling and optimization of 22-nm node SOI and BOI FinFET are performed including self-heating effects. The extracted subthreshold swing and DIBL justify the benefits of the non-planar structure in SCEs management. After the construction and calibration of both n-type and p-type devices, the transistors are implemented into the digital basic module for the performance evaluation. TCAD mixed-mode simulation results show that SHE is modest in both devices and during digital circuit DC operations. However, SOI FinFET SRAM memory module shows faster AC response because of smaller coupling capacitance between source/drain regions and the substrate. Design considerations along with TCAD simulation results recommend that SOI FinFET would be more preferable than BOI FinFET for the design of low-power digital circuits. Besides the investigation of FinFET

for volatile memory, a brief study has been conducted to evaluate the non-volatile memory SONOS FinFET cell, which shows a smaller operation voltage requirement and improved SCEs than the conventional planar counterpart.

The realization of FinFET for analog/RF functionalities can be achieved through the multi-fin configuration. The doping profile optimization guideline is developed for the compromise between analog/RF FoM and SCEs. With the consideration of extrinsic components through parasitic elements modeling, simulation results suggest that the optimized underlap design provides higher  $A_{VO}$  and  $f_{max}$  and maintain suppressed SCEs performance. The TCAD modeling also predicts that a large number of fins degrade the RF FoM but the underlap design has alleviated loss of high frequency performance.

For the III-V semiconductor technology, wide and narrow bandgap materials are investigated for non-digital and digital applications, respectively.

In this part, first, GaN, an emerging wide bandgap candidate to RF/analog applications is investigated via physics analysis and TCAD engineering. In this dissertation, the research efforts are on the lately proposed N-polar GaN material. We, for the first time, provide calibrated TCAD modeling of E-mode N-polar GaN single-channel HEMT for instance. Then through theoretical study of GaN HEMT on-resistance models and the specific feature of N-polar GaN material, a novel E-mode dual-channel hybrid MIS-HEMT is designed by the introduction of a surface inversion carrier channel in addition to the natural 2DEG close to the back barrier interface. The dual channel shows a low threshold voltage but more than two times of  $I_{max}$  compared to the single-channel MIS-HEMT. The impact of GaN scaling is also studied. Reducing GaN layer thickness



will improve the bottom 2DEG density but may cause channel overlap, which is demonstrated by TCAD prediction.

The other compound, InGaAs, is suitable for low-power high-performance applications because of its superior transport properties. Upper limit projections are made through the scaling of InGaAs planar and non-planar transistors. High current drivability is demonstrated for both structures while the non-planar InGaAs device shows better SCEs benefiting from the enhanced gate control.

By extensive research work on the non-classical transistors, this work has demonstrated that deep understanding provides foundation for TCAD simulation and device visualization while TCAD modeling provides the detailed physics insights and speeds up the investigation of novel devices development and optimization. The combination of numerical simulation and physics analysis conducted in this research work greatly promote the development of solid state electronics.

## **7.2 Suggestions for Future Research**

For silicon technology, as scaling of semiconductor device, process variations inevitably become a critical issue for ultra-small volume transistors. Line edge roughness (LER), inherent to various patterning steps, distorts device geometrical shape and affects its electrical behaviors. LER effect is due to the limit of lithography technology and it results in leakage degradation and threshold voltage variation [111]. Besides the structure problem, the random dopant fluctuation (RDF) effect also can lead to a dramatic increase in threshold voltage variation even for FinFET with a lightly doped body. The decreased impurity atoms in a tiny fin result in a random placement, contributing to the threshold voltage variation [112]. In a real nanoscale circuit module, when RDF interacts LER, the

circuit performance will be profoundly altered and the reliability of the whole IC will be detrimentally harmed. For an accurate prediction of variability, a 3-D Monte-Carlo atomistic simulation with an optimized statistical method is desired to quantify the variation distribution [52]. It should be noted that this comprehensive simulation demand huge amount of computation in a long term for data harvesting, data mining, and statistical analysis. Research efforts on the simulation efficiency while compromising accuracy and robustness will be welcomed by scientific community [113].

For III-V technology, although nitride electronics development has been booming recently, the progress of III-V devices, including both wide bandgap materials (GaN, AlN and AlGaIn) and narrow bandgap materials (InAs, InGaAs), has been hampered by electrically active defects that manifest as traps affecting device performance and reliability. To minimize those negative impacts and continue the advancement of III-V semiconductors, a fundamental understanding of the defects is indispensable and the correlations of defects to the performance and reliability degradation is required.

To speed up the exploration of trap effects, TCAD, the powerful gear, can be applied for a comprehensive understanding of III-V device electrical behaviors. In this dissertation work, trap impacts are given consideration for both GaN and InGaAs transistors. For GaN HEMT, bulk traps and interface traps are included to reflect the epi layers physical reality and calibrate threshold voltage and  $I_{\text{off}}$ . But for the surface traps, due to the rudimentary trap model and the correlated controversial physics explanation, the surface states and the resulting current collapse phenomena are not presented. It is recommended that the surface defects model should be developed based on the enhanced trap characterization techniques and convincing physics support. TCAD will also play an

important role in the model development and validation. The negative trap impact is considered as a critical challenge for InGaAs device as well. Although the ideal physics prediction and the TCAD modeling imply InGaAs can conduct high current under low bias, the high density interface states within the III-V transistor greatly reduce the free carrier and restrict the maximum performance. A reliable and robust trap model is expected for an accurate TCAD modeling. The development should be carried out with experimental measurement, modeling and TCAD calibration.

# Bibliography

- [1] J.-P. Colinge, "The SOI MOSFET: from Single Gate to Multigate," in *FinFETs and Other Multi-Gate Transistors*, J.-P. Colinge, Ed., ed: Springer US, 2008, pp. 1-48.
- [2] (2011). *International Technology Roadmap for Semiconductors*. Available: <http://www.itrs.net/Links/2011ITRS/Home2011.htm>
- [3] R. K. Cavin, P. Lugli, and V. V. Zhirnov, "Science and Engineering Beyond Moore's Law," *Proceedings of the IEEE*, vol. 100, pp. 1720-1749, 2012.
- [4] S. Borkar, "Design challenges of technology scaling," *Micro, IEEE*, vol. 19, pp. 23-29, 1999.
- [5] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and W. Hon-Sum Philip, "Device scaling limits of Si MOSFETs and their application dependencies," *Proceedings of the IEEE*, vol. 89, pp. 259-288, 2001.
- [6] T. Yuan, D. A. Buchanan, C. Wei, D. J. Frank, K. E. Ismail, L. Shih-Hsien, *et al.*, "CMOS scaling into the nanometer regime," *Proceedings of the IEEE*, vol. 85, pp. 486-504, 1997.
- [7] A. Asenov, S. Kaya, and J. H. Davies, "Intrinsic threshold voltage fluctuations in decanano MOSFETs due to local oxide thickness variations," *Electron Devices, IEEE Transactions on*, vol. 49, pp. 112-119, 2002.
- [8] N. G. Tarr, D. J. Walkey, M. B. Rowlandson, S. B. Hewitt, and T. W. MacElwee, "Short-channel effects on MOSFET subthreshold swing," *Solid-State Electronics*, vol. 38, pp. 697-701, 1995.
- [9] Q. Xie, J. Xu, and Y. Taur, "Review and Critique of Analytic Models of MOSFET Short-Channel Effects in Subthreshold," *Electron Devices, IEEE Transactions on*, vol. 59, pp. 1569-1579, 2012.
- [10] E. P. Vandamme, P. Jansen, and L. Deferm, "Modeling the subthreshold swing in MOSFET's," *Electron Device Letters, IEEE*, vol. 18, pp. 369-371, 1997.
- [11] R. R. Troutman, "VLSI limitations from drain-induced barrier lowering," *Electron Devices, IEEE Transactions on*, vol. 26, pp. 461-469, 1979.
- [12] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, "On the universality of inversion layer mobility in Si MOSFET's: Part II-effects of surface orientation," *Electron Devices, IEEE Transactions on*, vol. 41, pp. 2363-2368, 1994.
- [13] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proceedings of the IEEE*, vol. 91, pp. 305-327, 2003.
- [14] P. Oldiges, K. Bernstein, D. Heidel, B. Klaasen, E. Cannon, R. Dennard, *et al.*, "Soft error rate scaling for emerging SOI technology options," in *VLSI Technology, 2002. Digest of Technical Papers. 2002 Symposium on*, 2002, pp. 46-47.
- [15] (2003). *Intel's High-k/Metal Gate Announcement*. Available: <http://download.intel.com/technology/silicon/HighK-MetalGate-PressFoil-final.pdf>

- [16] C. Auth, A. Cappellani, J. S. Chun, A. Dalis, A. Davis, T. Ghani, *et al.*, "45nm High-k + metal gate strain-enhanced transistors," in *VLSI Technology, 2008 Symposium on*, 2008, pp. 128-129.
- [17] X. Chen, S. Samavedam, V. Narayanan, K. Stein, C. Hobbs, C. Baiocco, *et al.*, "A cost effective 32nm high-K/ metal gate CMOS technology for low power applications with single-metal/gate-first process," in *VLSI Technology, 2008 Symposium on*, 2008, pp. 88-89.
- [18] Y. Nara, "Scaling challenges of MOSFET for 32nm node and beyond," in *VLSI Technology, Systems, and Applications, 2009. VLSI-TSA '09. International Symposium on*, 2009, pp. 72-73.
- [19] (2010). "More-than-Moore" White Paper Available: <http://www.itrs.net/Links/2010ITRS/IRC-ITRS-MtM-v2%203.pdf>
- [20] (2010). *International Technology Roadmap for Semiconductors*. Available: <http://www.itrs.net/Links/2011ITRS/Home2011.htm>
- [21] (2011). *Introducing the World's first 3-D Transistor Ready for High-volume Manufacturing*. Available: <http://www.intel.com/content/www/us/en/silicon-innovations/intel-22nm-technology.html>
- [22] *Multigate Device*. Available: Multigate device
- [23] K. Dae-Hyun, J. A. del Alamo, L. Jae-Hak, and S. Kwang-Seok, "Logic Suitability of 50-nm In<sub>0.7</sub>Ga<sub>0.3</sub>As HEMTs for Beyond-CMOS Applications," *Electron Devices, IEEE Transactions on*, vol. 54, pp. 2606-2613, 2007.
- [24] M. Radosavljevic, G. Dewey, J. M. Fastenau, J. Kavalieros, R. Kotlyar, B. Chu-Kung, *et al.*, "Non-planar, multi-gate InGaAs quantum well field effect transistors with high-K gate dielectric and ultra-scaled gate-to-drain/gate-to-source separation for low power logic applications," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, 2010, pp. 6.1.1-6.1.4.
- [25] M. Radosavljevic, G. Dewey, D. Basu, J. Boardman, B. Chu-Kung, J. M. Fastenau, *et al.*, "Electrostatics improvement in 3-D tri-gate over ultra-thin body planar InGaAs quantum well field effect transistors with high-K gate dielectric and scaled gate-to-drain/gate-to-source separation," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, pp. 33.1.1-33.1.4.
- [26] S. Oh and H. P. Wong, "Viability Study of All-III-V SRAM for Beyond-22-nm Logic Circuits," *Electron Device Letters, IEEE*, vol. 32, pp. 877-879, 2011.
- [27] U. K. Mishra, L. Shen, T. E. Kazior, and W. Yi-Feng, "GaN-Based RF Power Devices and Amplifiers," *Proceedings of the IEEE*, vol. 96, pp. 287-305, 2008.
- [28] D. C. Cole, E. M. Buturla, S. S. Furkay, K. Varahramyan, J. Slinkman, J. A. Mandelman, *et al.*, "The use of simulation in semiconductor technology development," *Solid-State Electronics*, vol. 33, pp. 591-623, 1990.
- [29] G. A. Armstrong and C. K. Maiti, "Introduction," in *TCAD for Si, SiGe and GaAs Integrated Circuits*, ed, 2007.
- [30] T. Ma, V. Moroz, R. Borges, and L. Smith, "TCAD: Present state and future challenges," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, 2010, pp. 15.3.1-15.3.4.
- [31] *Mesh Generation Tools User Guide (F-2011.09 ed.)*. Available: [www.synopsys.com](http://www.synopsys.com)
- [32] *Sentaurus Device User Guide (F-2011.09 ed.)*. Available: [www.synopsys.com](http://www.synopsys.com)

- [33] E. Buturla, "The use of TCAD in semiconductor technology development," in *Custom Integrated Circuits Conference, 1991., Proceedings of the IEEE 1991*, 1991, pp. 23.1/1-23.1/7.
- [34] R. W. Dutton and M. R. Pinto, "The use of computer aids in IC technology evolution," *Proceedings of the IEEE*, vol. 74, pp. 1730-1740, 1986.
- [35] T. Skotnicki, G. Merckel, and T. Pedron, "The voltage-doping transformation: a new approach to the modeling of MOSFET short-channel effects," *Electron Device Letters, IEEE*, vol. 9, pp. 109-112, 1988.
- [36] T. Skotnicki, "Heading for decanometer CMOS - Is navigation among icebergs still a viable strategy?," in *Solid-State Device Research Conference, 2000. Proceeding of the 30th European*, 2000, pp. 19-33.
- [37] A. Asenov, A. R. Brown, J. H. Davies, S. Kaya, and G. Slavcheva, "Simulation of intrinsic parameter fluctuations in decanometer and nanometer-scale MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 50, pp. 1837-1852, 2003.
- [38] K. Itoh, N. Sugii, D. Hisamoto, and R. Tsuchiya, "FD-SOI MOSFETs for the low-voltage nanoscale CMOS era," in *SOI Conference, 2009 IEEE International*, 2009, pp. 1-4.
- [39] H. Sasaki, M. Ono, T. Yoshitomi, T. Ohguro, S. Nakamura, M. Saito, *et al.*, "1.5 nm direct-tunneling gate oxide Si MOSFET's," *Electron Devices, IEEE Transactions on*, vol. 43, pp. 1233-1242, 1996.
- [40] S. Balasubramanian, "Nanoscale thin-body MOSFET design and applications," Dissertation, University of California at Berkeley, 2006.
- [41] D. Hisamoto, L. Wen-Chin, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, *et al.*, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *Electron Devices, IEEE Transactions on*, vol. 47, pp. 2320-2325, 2000.
- [42] Y. Bin, C. Leland, S. Ahmed, W. Haihong, S. Bell, Y. Chih-Yuh, *et al.*, "FinFET scaling to 10 nm gate length," in *Electron Devices Meeting, 2002. IEDM '02. International*, 2002, pp. 251-254.
- [43] Y. Fu-Liang, L. Di-Hong, C. Hou-Yu, C. Chang-Yun, L. Sheng-Da, H. Cheng-Chuan, *et al.*, "5nm-gate nanowire FinFET," in *VLSI Technology, 2004. Digest of Technical Papers. 2004 Symposium on*, 2004, pp. 196-197.
- [44] L. Hyunjin, Y. Lee-Eun, R. Seong-Wan, H. Jin-Woo, J. Kanghoon, J. Dong-Yoon, *et al.*, "Sub-5nm All-Around Gate FinFET for Ultimate Scaling," in *VLSI Technology, 2006. Digest of Technical Papers. 2006 Symposium on*, 2006, pp. 58-59.
- [45] S. H. Tang, L. Chang, N. Lindert, C. Yang-Kyu, L. Wen-Chin, H. Xuejue, *et al.*, "FinFET-a quasi-planar double-gate MOSFET," in *Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International*, 2001, pp. 118-119, 437.
- [46] L. Chang, C. Yang-kyu, D. Ha, P. Ranade, X. Shiyang, J. Bokor, *et al.*, "Extremely scaled silicon nano-CMOS devices," *Proceedings of the IEEE*, vol. 91, pp. 1860-1873, 2003.
- [47] S. Jooyoung, Y. Bo, Y. Yu, and T. Yuan, "A Review on Compact Modeling of Multiple-Gate MOSFETs," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 56, pp. 1858-1869, 2009.

- [48] H. Xuejue, L. Wen-Chin, C. Kuo, D. Hisamoto, C. Leland, J. Kedzierski, *et al.*, "Sub-50 nm P-channel FinFET," *Electron Devices, IEEE Transactions on*, vol. 48, pp. 880-886, 2001.
- [49] T. Park, S. Choi, D. H. Lee, J. R. Yoo, B. C. Lee, J. Y. Kim, *et al.*, "Fabrication of body-tied FinFETs (Omega MOSFETs) using bulk Si wafers," in *VLSI Technology, 2003. Digest of Technical Papers. 2003 Symposium on*, 2003, pp. 135-136.
- [50] P. Jong-Man, H. Sang-Yeon, J. Chang-Hoon, S. Si-Ok, L. Jun-Bum, S. Yamada, *et al.*, "Fully Integrated Advanced Bulk FinFETs Architecture Featuring Partially-Insulating Technique for DRAM Cell Application of 40nm Generation and Beyond," in *Electron Devices Meeting, 2006. IEDM '06. International*, 2006, pp. 1-4.
- [51] P. Tai-Su, C. Hye Jin, C. Jeong Dong, H. Sang Yeon, P. Donggun, K. Kinam, *et al.*, "Characteristics of the full CMOS SRAM cell using body-tied TG MOSFETs (bulk FinFETs)," *Electron Devices, IEEE Transactions on*, vol. 53, pp. 481-487, 2006.
- [52] W. Xingsheng, A. R. Brown, C. Binjie, and A. Asenov, "Statistical variability and reliability in nanoscale FinFETs," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, pp. 5.4.1-5.4.4.
- [53] X. Xiaoyan, W. Runsheng, H. Ru, Z. Jing, C. Gang, Z. Xing, *et al.*, "High-Performance BOI FinFETs Based on Bulk-Silicon Substrate," *Electron Devices, IEEE Transactions on*, vol. 55, pp. 3246-3250, 2008.
- [54] D. M. F. Horacio Mendez, Srikanth B. Samavedam, Thomas Hoffmann, Bich-Yen Nguyen. (2009, Comparing SOI and bulk FinFETs: Performance, manufacturing variability, and cost. *Solid State Technology* 52(11).
- [55] T. Chiarella, L. Witters, A. Mercha, C. Kerner, R. Dittrich, M. Rakowski, *et al.*, "Migrating from planar to FinFET for further CMOS scaling: SOI or bulk?," in *ESSCIRC, 2009. ESSCIRC '09. Proceedings of*, 2009, pp. 84-87.
- [56] M. Guillorn, J. Chang, A. Bryant, N. Fuller, O. Dokumaci, X. Wang, *et al.*, "FinFET performance advantage at 22nm: An AC perspective," in *VLSI Technology, 2008 Symposium on*, 2008, pp. 12-13.
- [57] C. Chang-Yun, L. Tsung-Lin, C. Wann, L. Li-Shyue, C. Hung-Ming, Y. Chih-Chieh, *et al.*, "A 25-nm gate-length FinFET transistor module for 32nm node," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.
- [58] H. Kawasaki, V. S. Basker, T. Yamashita, C. H. Lin, Y. Zhu, J. Faltermeier, *et al.*, "Challenges and solutions of FinFET integration in an SRAM cell and a logic circuit for 22 nm node and beyond," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.
- [59] R. C. Jaeger and T. N. Blalock, "SRAM," *Microelectronic Circuit Design*, p. 402, 2010.
- [60] C. Fiegna, Y. Yang, E. Sangiorgi, and A. G. O'Neill, "Analysis of Self-Heating Effects in Ultrathin-Body SOI MOSFETs by Device Simulation," *Electron Devices, IEEE Transactions on*, vol. 55, pp. 233-244, 2008.
- [61] R. C. Jaeger and T. Blalock, "Static Memory Cells," in *Microelectronic Circuit Design*, 4 ed: McGraw-Hill, 2010, pp. 419-428.

- [62] A. Bansal, S. Mukhopadhyay, and K. Roy, "Device-Optimization Technique for Robust and Low-Power FinFET SRAM Design in NanoScale Era," *Electron Devices, IEEE Transactions on*, vol. 54, pp. 1409-1419, 2007.
- [63] E. Seevinck, F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," *Solid-State Circuits, IEEE Journal of*, vol. 22, pp. 748-754, 1987.
- [64] G. Zheng, S. Balasubramanian, R. Zlatanovici, K. Tsu-Jae, and B. Nikolic, "FinFET-based SRAM design," in *Low Power Electronics and Design, 2005. ISLPED '05. Proceedings of the 2005 International Symposium on*, 2005, pp. 2-7.
- [65] C. Y. Hsieh, M. L. Fan, V. P. H. Hu, P. Su, and C. T. Chuang, "Independently-Controlled-Gate FinFET Schmitt Trigger Sub-Threshold SRAMs," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. PP, pp. 1-10, 2011.
- [66] R. Kapre, K. Shakeri, H. Puchner, J. Tandigan, T. Nigam, K. Jang, *et al.*, "SRAM Variability and Supply Voltage Scaling Challenges," in *Reliability physics symposium, 2007. proceedings. 45th annual. ieee international*, 2007, pp. 23-28.
- [67] H. Ananthan, A. Bansal, and K. Roy, "FinFET SRAM - device and circuit design considerations," in *Quality Electronic Design, 2004. Proceedings. 5th International Symposium on*, 2004, pp. 511-516.
- [68] S. M. Sze and K. K. Ng, "Nonvolatile Memory Device," *Physics of Semiconductor Devices*, p. 350, 2007.
- [69] J. Bu and M. H. White, "Design considerations in scaled SONOS nonvolatile memory devices," *Solid-State Electronics*, vol. 45, pp. 113-120, 2001.
- [70] M. H. White, D. A. Adams, and J. Bu, "On the go with SONOS," *Circuits and Devices Magazine, IEEE*, vol. 16, pp. 22-31, 2000.
- [71] B. Eitan and D. Frohman-Bentchkowsky, "Hot-electron injection into the oxide in n-channel MOS devices," *Electron Devices, IEEE Transactions on*, vol. 28, pp. 328-340, 1981.
- [72] M. Lenzlinger and E. H. Snow, "Fowler-Nordheim Tunneling into Thermally Grown SiO<sub>2</sub>," *Journal of Applied Physics*, vol. 40, pp. 278-283, 1969.
- [73] H. Tzu-Hsuan, L. Hang-Ting, L. Sheng-Chih, K. Ya-Chin, H. Kuang-Yeu, L. Rich, *et al.*, "Reliability of planar and FinFET SONOS devices for NAND flash applications - Field enhancement vs. barrier engineering," in *VLSI Technology, Systems, and Applications, 2009. VLSI-TSA '09. International Symposium on*, 2009, pp. 154-155.
- [74] M. H. White, Y. Yang, P. Ansha, and M. L. French, "A low voltage SONOS nonvolatile semiconductor memory technology," *Components, Packaging, and Manufacturing Technology, Part A, IEEE Transactions on*, vol. 20, pp. 190-195, 1997.
- [75] W. Xuguang and K. Dim-Lee, "A novel high- $\kappa$ ; SONOS memory using TaN/Al<sub>2</sub>O<sub>3</sub>/Ta<sub>2</sub>O<sub>5</sub>/HfO<sub>2</sub>/Si structure for fast speed and long retention operation," *Electron Devices, IEEE Transactions on*, vol. 53, pp. 78-82, 2006.
- [76] M. L. French and M. H. White, "Scaling of multielectric nonvolatile SONOS memory structures," *Solid-State Electronics*, vol. 37, pp. 1913-1923, 1994.
- [77] L. Dong Hua, P. Il Han, C. Seongjae, Y. Jang-Gn, L. Jung Hoon, K. Doo-Hyun, *et al.*, "Effects of equivalent oxide thickness on bandgap-engineered SONOS flash memory," in *Nanotechnology Materials and Devices Conference, 2009. NMDC '09. IEEE*, 2009, pp. 255-258.



- [78] A. Kranti, J. P. Raskin, and G. A. Armstrong, "Optimizing FinFET geometry and parasitics for RF applications," in *SOI Conference, 2008. SOI. IEEE International*, 2008, pp. 123-124.
- [79] V. Subramanian, A. Mercha, B. Parvais, M. Dehan, G. Groeseneken, W. Sansen, *et al.*, "Identifying the Bottlenecks to the RF Performance of FinFETs," in *VLSI Design, 2010. VLSID '10. 23rd International Conference on*, 2010, pp. 111-116.
- [80] A. Kranti and G. A. Armstrong, "Design and Optimization of FinFETs for Ultra-Low-Voltage Analog Applications," *Electron Devices, IEEE Transactions on*, vol. 54, pp. 3308-3316, 2007.
- [81] V. Trivedi, J. G. Fossum, and M. M. Chowdhury, "Nanoscale FinFETs with gate-source/drain underlap," *Electron Devices, IEEE Transactions on*, vol. 52, pp. 56-62, 2005.
- [82] Y. Ji-Woon, P. M. Zeitzoff, and T. Hsing-Huang, "Highly Manufacturable Double-Gate FinFET With Gate-Source/Drain Underlap," *Electron Devices, IEEE Transactions on*, vol. 54, pp. 1464-1470, 2007.
- [83] I. Young, "MOSFET Extrinsic Parasitic Elements - Short Course," in *Electron Devices Meeting (IEDM), 2010 IEEE International*, Washington D. C., 2011.
- [84] J. P. Raskin, G. Pailloncy, D. Lederer, F. Danneville, G. Dambrine, S. Decoutere, *et al.*, "High-Frequency Noise Performance of 60-nm Gate-Length FinFETs," *Electron Devices, IEEE Transactions on*, vol. 55, pp. 2718-2727, 2008.
- [85] W. Kuang, "TCAD simulation and modeling of aluminum gallium nitride/gallium nitride HFETs," Ph.D. 3395217, North Carolina State University, United States -- North Carolina, 2008.
- [86] O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, *et al.*, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N- and Ga-face AlGaIn/GaN heterostructures," *Journal of Applied Physics*, vol. 85, pp. 3222-3233, 1999.
- [87] C. Wood and D. Jena, "Polarization Effects on Low-Field Transport & Mobility in III-V Nitride HEMTs," in *Polarization Effects in Semiconductors: From Ab Initio Theory to Device Applications*, ed: Springer, 2007.
- [88] U. K. Mishra and J. Singh, "Field Effect Transistors," in *Semiconductor Device Physics and Design*, ed: Springer, 2008.
- [89] Y. F. Wu, A. Saxler, M. Moore, R. P. Smith, S. Sheppard, P. M. Chavarkar, *et al.*, "30-W/mm GaN HEMTs by field plate optimization," *Electron Device Letters, IEEE*, vol. 25, pp. 117-119, 2004.
- [90] W. Yi-Feng, D. Kapolnek, J. P. Ibbetson, P. Parikh, B. P. Keller, and U. K. Mishra, "Very-high power density AlGaIn/GaN HEMTs," *Electron Devices, IEEE Transactions on*, vol. 48, pp. 586-590, 2001.
- [91] S. T. Sheppard, K. Doverspike, W. L. Pribble, S. T. Allen, J. W. Palmour, L. T. Kehias, *et al.*, "High-power microwave GaN/AlGaIn HEMTs on semi-insulating silicon carbide substrates," *Electron Device Letters, IEEE*, vol. 20, pp. 161-163, 1999.
- [92] D. F. Brown, A. Williams, K. Shinohara, A. Kurdoghlian, I. Milosavljevic, P. Hashimoto, *et al.*, "W-band power performance of AlGaIn/GaN DHFETs with regrown n+ GaN ohmic contacts by MBE," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, pp. 19.3.1-19.3.4.

- [93] A. L. Corrion, K. Shinohara, D. Regan, I. Milosavljevic, P. Hashimoto, P. J. Willadsen, *et al.*, "Enhancement-Mode AlN/GaN/AlGaN DHFET With 700-mS/mm  $g_m$  and 112-GHz  $f_T$ ," *Electron Device Letters, IEEE*, vol. 31, pp. 1116-1118, 2010.
- [94] S. Haifeng, A. R. Alt, H. Benedickter, E. Feltin, J. F. Carlin, M. Gonschorek, *et al.*, "205-GHz (Al,In)N/GaN HEMTs," *Electron Device Letters, IEEE*, vol. 31, pp. 957-959, 2010.
- [95] T. Imada, M. Kanamura, and T. Kikkawa, "Enhancement-mode GaN MIS-HEMTs for power supplies," in *Power Electronics Conference (IPEC), 2010 International*, 2010, pp. 1027-1033.
- [96] U. Singiseti, W. Man Hoi, J. S. Speck, and U. K. Mishra, "Enhancement-Mode N-Polar GaN MOS-HFET With 5-nm GaN Channel, 510-mS/mm  $g_m$ , and 0.66  $\Omega$ mm  $R_{on}$ ," *Electron Device Letters, IEEE*, vol. 33, pp. 26-28, 2012.
- [97] U. Singiseti, W. Man Hoi, S. Dasgupta, Nidhi, B. Swenson, B. J. Thibeault, *et al.*, "Enhancement-Mode N-Polar GaN MISFETs With Self-Aligned Source/Drain Regrowth," *Electron Device Letters, IEEE*, vol. 32, pp. 137-139, 2011.
- [98] S. Kolluri, P. Yi, S. Keller, S. P. Denbaars, and U. K. Mishra, "RF Performance of N-Polar AlGaIn/GaN MIS-HEMT Grown by MOCVD on Sapphire Substrate," *Electron Device Letters, IEEE*, vol. 30, pp. 584-586, 2009.
- [99] J. W. Chung, E. L. Piner, and T. Palacios, "N-Face GaN/AlGaIn HEMTs Fabricated Through Layer Transfer Technology," *Electron Device Letters, IEEE*, vol. 30, pp. 113-116, 2009.
- [100] S. Dasgupta, Nidhi, D. F. Brown, F. Wu, S. Keller, J. S. Speck, *et al.*, "Ultralow nonalloyed Ohmic contact resistance to self aligned N-polar GaN high electron mobility transistors by In(Ga)N regrowth," *Applied Physics Letters*, vol. 96, pp. 143504-143504-3, 2010.
- [101] M. H. Wong, Y. Pei, T. Palacios, L. Shen, A. Chakraborty, L. S. McCarthy, *et al.*, "Low nonalloyed Ohmic contact resistance to nitride high electron mobility transistors using N-face growth," *Applied Physics Letters*, vol. 91, pp. 232103-3, 2007.
- [102] S. Kolluri, S. Keller, S. P. DenBaars, and U. K. Mishra, "N-Polar GaN MIS-HEMTs With a 12.1-W/mm Continuous-Wave Output Power Density at 4 GHz on Sapphire Substrate," *Electron Device Letters, IEEE*, vol. 32, pp. 635-637, 2011.
- [103] K. Nomoto, T. Tajima, T. Mishima, M. Satoh, and T. Nakamura, "Remarkable Reduction of On-Resistance by Ion Implantation in GaN/AlGaIn/GaN HEMTs With Low Gate Leakage Current," *Electron Device Letters, IEEE*, vol. 28, pp. 939-941, 2007.
- [104] Y. Hayashi, S. Sugiura, S. Kishimoto, and T. Mizutani, "AlGaIn/GaN MOSHFETs with HfO<sub>2</sub> gate oxide: A simulation study," *Solid-State Electronics*, vol. 54, pp. 1367-1371, 2010.
- [105] Y. Xuan, Y. Q. Wu, H. C. Lin, T. Shen, and P. D. Ye, "Submicrometer Inversion-Type Enhancement-Mode InGaAs MOSFET With Atomic-Layer-Deposited Al<sub>2</sub>O<sub>3</sub> as Gate Dielectric," *Electron Device Letters, IEEE*, vol. 28, pp. 935-938, 2007.

- [106] Y. Xuan, Y. Q. Wu, and P. D. Ye, "High-Performance Inversion-Type Enhancement-Mode InGaAs MOSFET With Maximum Drain Current Exceeding 1 A/mm," *Electron Device Letters, IEEE*, vol. 29, pp. 294-296, 2008.
- [107] C. Hock-Chun, G. Xiao, L. Xinke, L. Zhe, and Y. Yee-Chia, "Strained In<sub>0.53</sub>Ga<sub>0.47</sub>As n-MOSFETs: Performance boost with in-situ doped lattice-mismatched source/drain stressors and interface engineering," in *VLSI Technology, 2009 Symposium on*, 2009, pp. 244-245.
- [108] Y. Q. Wu, R. S. Wang, T. Shen, J. J. Gu, and P. D. Ye, "First experimental demonstration of 100 nm inversion-mode InGaAs FinFET through damage-free sidewall etching," in *Electron Devices Meeting (IEDM), 2009 IEEE International*, 2009, pp. 1-4.
- [109] M. Yokoyama, R. Iida, K. Sanghyeon, N. Taoka, Y. Urabe, H. Takagi, *et al.*, "Sub-10-nm Extremely Thin Body InGaAs-on-Insulator MOSFETs on Si Wafers With Ultrathin Al<sub>2</sub>O<sub>3</sub> Buried Oxide Layers," *Electron Device Letters, IEEE*, vol. 32, pp. 1218-1220, 2011.
- [110] U. Singiseti, M. A. Wistey, G. J. Burek, A. K. Baraskar, B. J. Thibeault, A. C. Gossard, *et al.*, "In<sub>0.53</sub>Ga<sub>0.47</sub>As Channel MOSFETs With Self-Aligned Source/Drain Formed by MEE Regrowth," *Electron Device Letters, IEEE*, vol. 30, pp. 1128-1130, 2009.
- [111] E. Baravelli, M. Jurczak, N. Speciale, K. De Meyer, and A. Dixit, "Impact of LER and Random Dopant Fluctuations on FinFET Matching Performance," *Nanotechnology, IEEE Transactions on*, vol. 7, pp. 291-298, 2008.
- [112] Y. Yun, F. Liu, C. Min, S. Nassif, and C. Yu, "Statistical Modeling and Simulation of Threshold Variation Under Random Dopant Fluctuations and Line-Edge Roughness," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 19, pp. 987-996, 2011.
- [113] D. Reid, C. Millar, S. Roy, and A. Asenov, "Statistical Enhancement of the Evaluation of Combined RDD- and LER-Induced V<sub>T</sub> Variability: Lessons From 10<sup>5</sup> Sample Simulations," *Electron Devices, IEEE Transactions on*, vol. 58, pp. 2257-2265, 2011.

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